

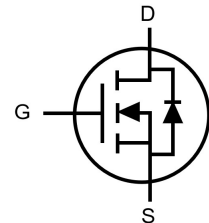
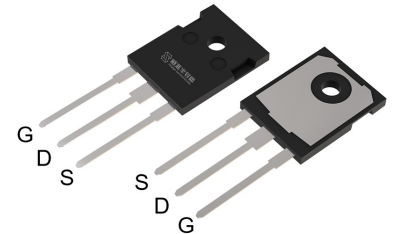
Features

- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=10\text{ V}$
- Super Junction Technology
- 100% Avalanche test, 100% Rg Tested



Part ID	Package Type	Marking	Packing
VSU070N65HS3	TO-247	070N65H	30pcs/Tube

V_{DS}	650	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	60	m Ω
$I_{D(Silicon\ Limited)}$	52	A

TO-247


Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	650	V
V_{GS}	Gate-Source voltage	± 30	V
I_S	Diode continuous forward current (Silicon limited)	$T_C = 25^\circ\text{C}$ 52	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$ 52	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$ 33	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 120	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$ 4.7	A
		$T_A = 70^\circ\text{C}$ 3.8	A
E_{AS}	Avalanche energy, single pulsed ②	1620	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$ 391	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$ 3.3	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.27	0.32	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	32	38	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =600V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C) ^⑦	V _{DS} =520V, V _{GS} =0V	--	--	50	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.3	2.8	3.3	V
R _{DS(on)}	Drain-Source On-State Resistance ^⑧	V _{GS} =10V, I _D =20A	--	60	70	mΩ
		T _j =100°C ^⑦	--	91	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ^⑦	V _{DS} =400V, V _{GS} =0V, f=250kHz	--	3140	--	pF
C _{oss}	Output Capacitance ^⑦		--	85	--	pF
C _{rss}	Reverse Transfer Capacitance ^⑦		--	4	--	pF
R _g	Gate Resistance	f=1MHz	--	0.7	--	Ω
Q _g	Total Gate Charge ^⑦	V _{DS} =400V, I _D =20A, V _{GS} =10V	--	78	--	nC
Q _{gs}	Gate-Source Charge ^⑦		--	15	--	nC
Q _{gd}	Gate-Drain Charge ^⑦		--	31	--	nC
Switching Characteristics ^⑦						
T _{d(on)}	Turn-on Delay Time	V _{DD} =400V, I _D =20A, R _G =10Ω, V _{GS} =10V	--	21	--	ns
T _r	Turn-on Rise Time		--	29	--	ns
T _{d(off)}	Turn-Off Delay Time		--	113	--	ns
T _f	Turn-Off Fall Time		--	41	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time ^⑦	I _{sd} =20A, V _{GS} =0V	--	356	--	ns
Q _{rr}	Reverse Recovery Charge ^⑦	di/dt=100A/μs	--	6.5	--	uC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② EAS of 1620mJ is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} = 10V; 100% FT tested at L = 10mH, I_{AS} = 9A.
- ③ The power dissipation P_d is based on T_j(max), using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_j(max), using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad).
- ⑥ The value of R_{θJA} is measured with the device in a still air environment with T_A = 25° C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

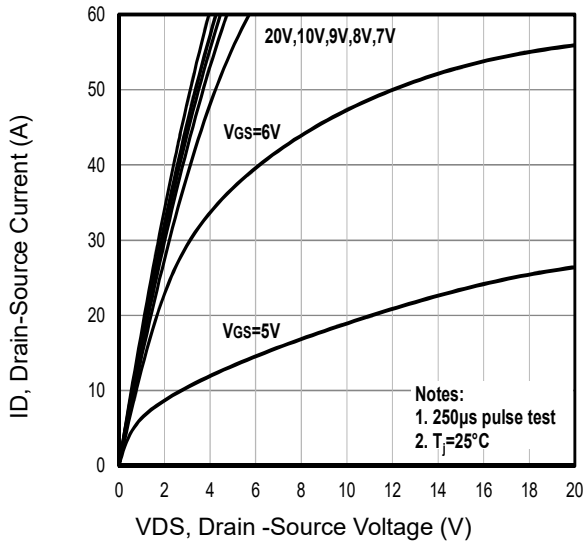


Fig1. Typical Output Characteristics

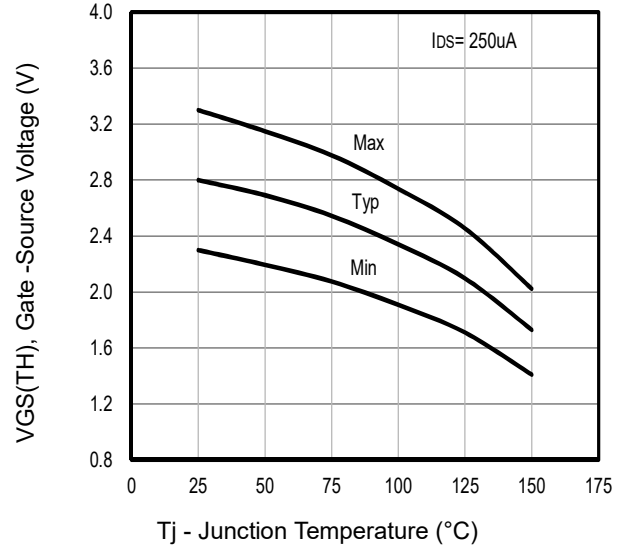


Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

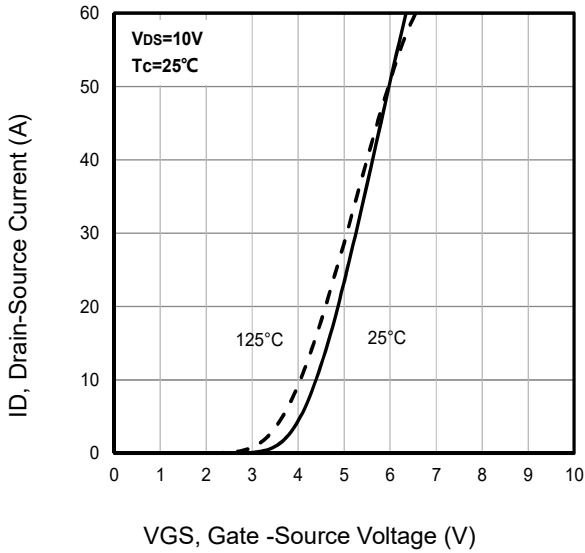


Fig3. Typical Transfer Characteristics

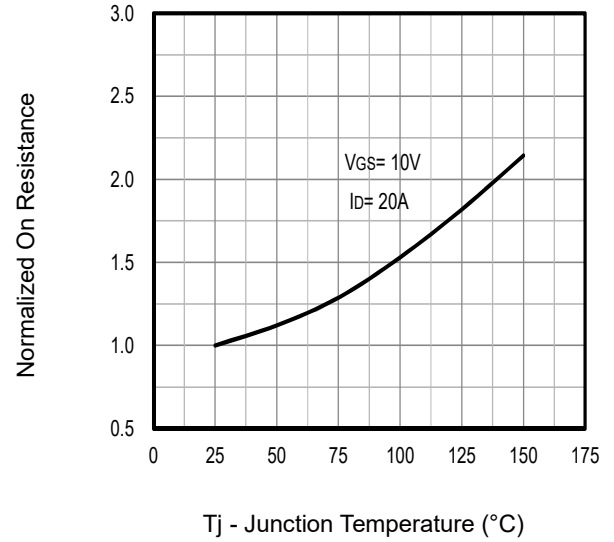


Fig4. Typical Normalized On-Resistance Vs. T_j

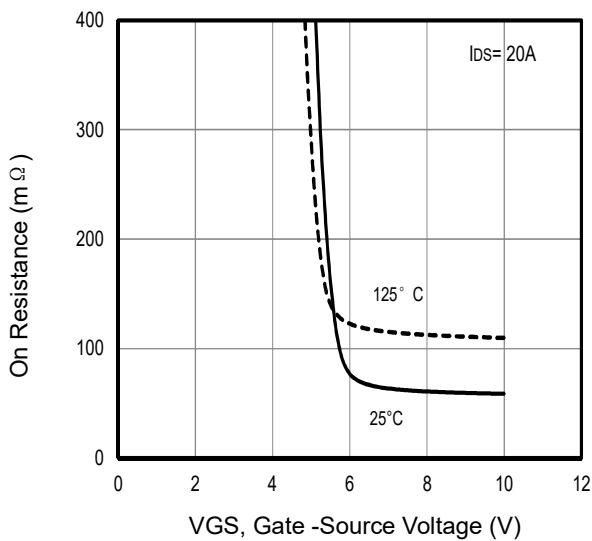


Fig5. Typical On Resistance Vs Gate-Source Voltage

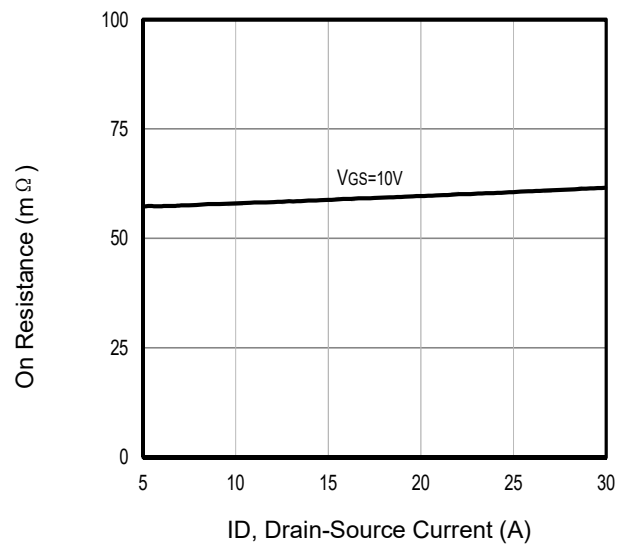


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

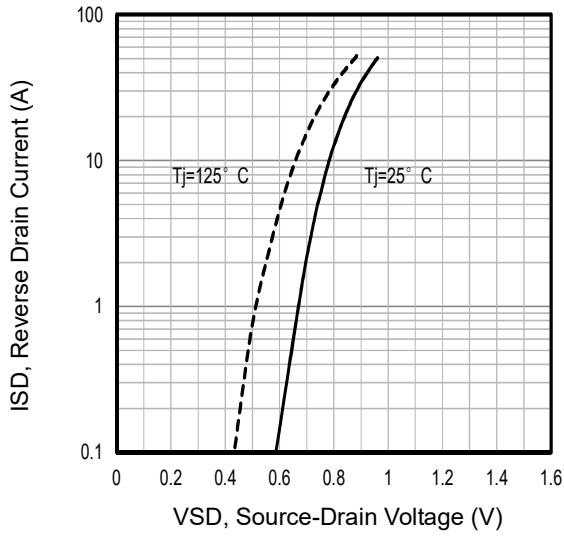


Fig7. Typical Source-Drain Diode Forward Voltage

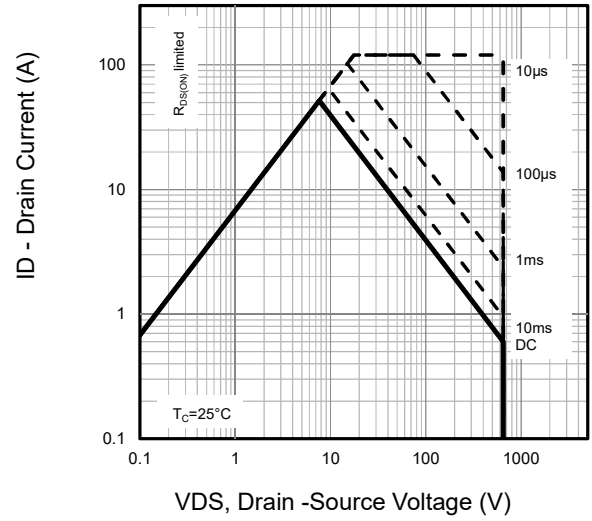


Fig8. Maximum Safe Operating Area

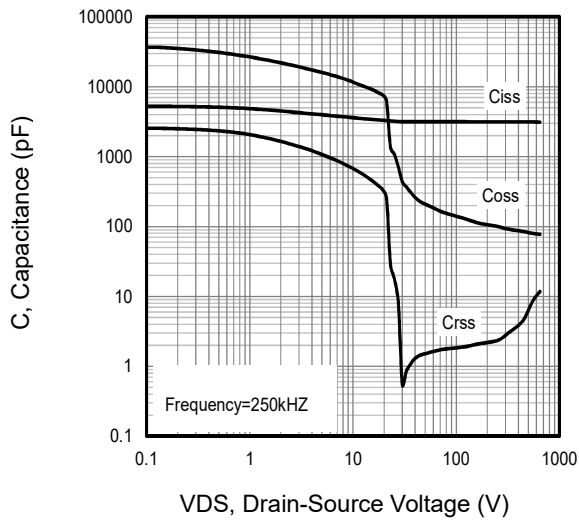


Fig9. Typical Capacitance Vs. Drain-Source Voltage

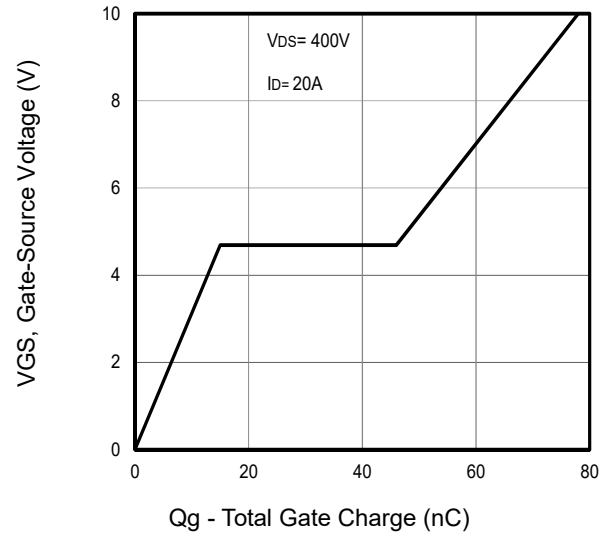


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

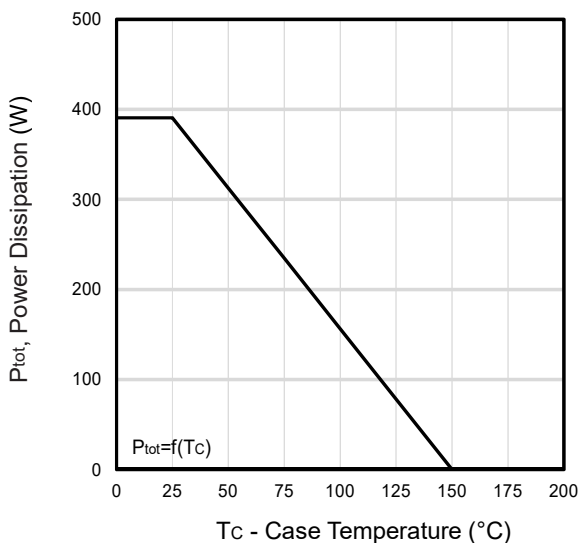


Fig11. Power Dissipation Vs. Case Temperature

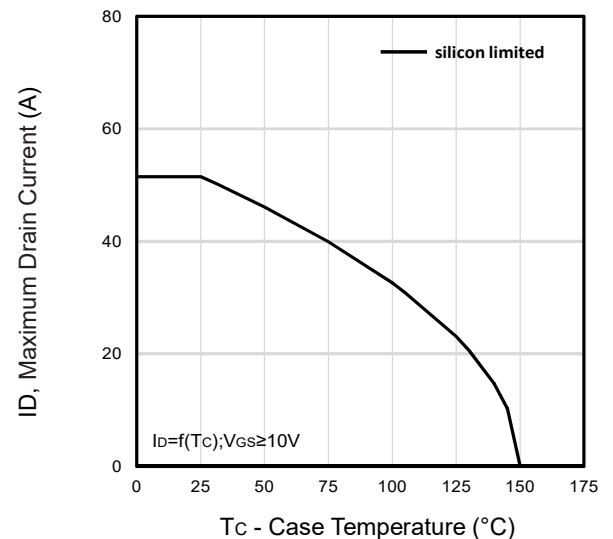


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

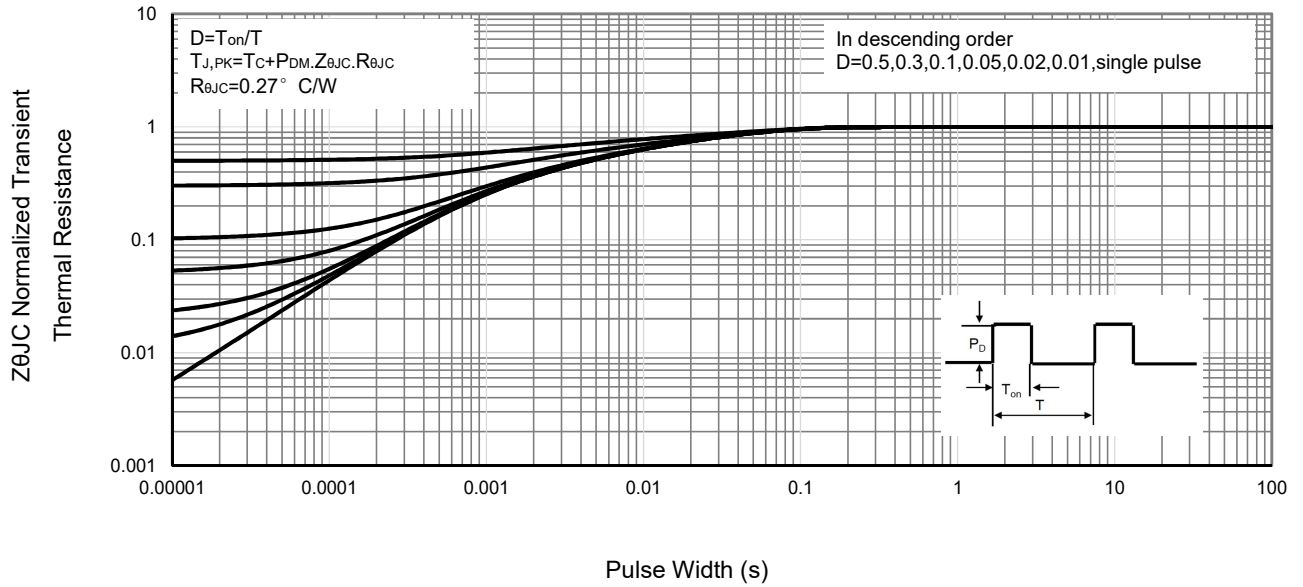


Fig13 . Normalized Maximum Transient Thermal Impedance

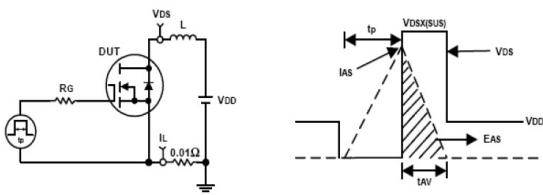


Fig14. Unclamped Inductive Test Circuit and waveforms

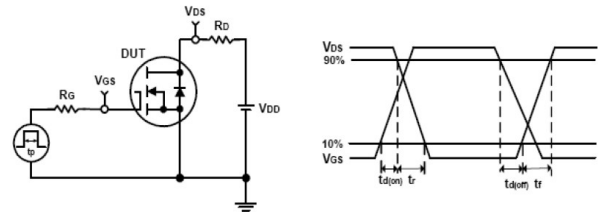
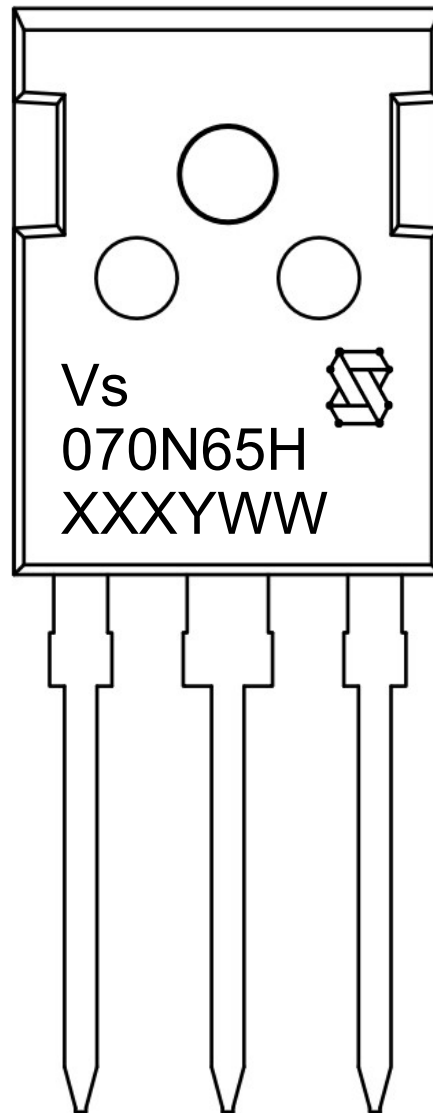


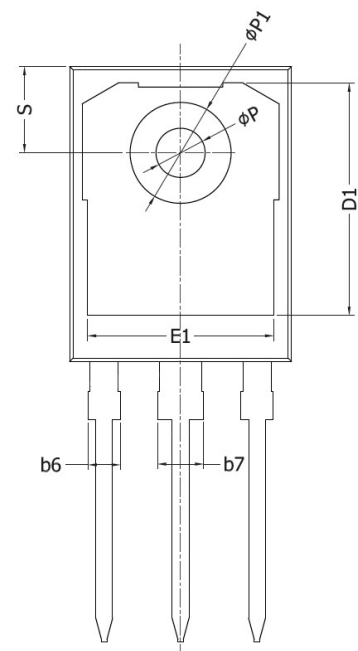
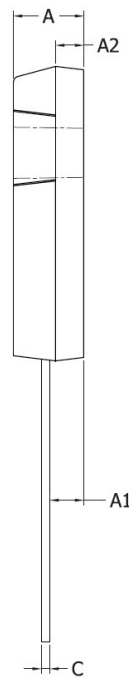
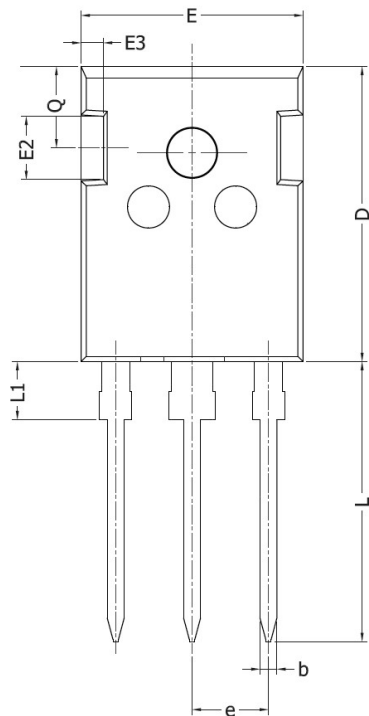
Fig15. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs) , Vergiga Logo
- 2nd line: Part Number (070N65H)
- 3rd line: Date code (XXXYWW)
 - XXX: Wafer Lot Number Code , code changed with Lot Number
 - Y: Year Code , refer to table below
 - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Nom	Max
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b6	1.91	--	2.21
b7	2.91	--	3.21
C	0.51	0.61	0.75
D	20.80	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.40	--	5.20
E3	1.50	1.60	1.70
e	5.44 BSC		
L	19.80	19.92	20.22
L1	--	--	4.30
ΦP	3.40	3.60	3.80
ΦP1	7.00	--	7.40
Q	5.60	5.80	6.00
S	6.05	6.15	6.25

Notes:

1. Package Reference: JEDEC TO-247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.

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