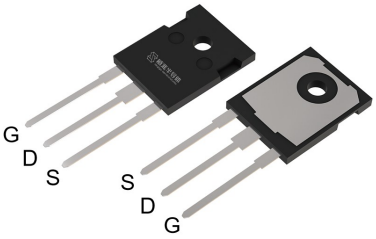
Features

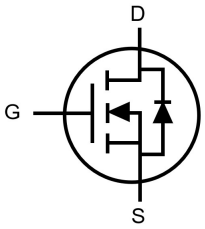
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=10 V
- Super Junction Technology
- 100% Avalanche test

V_{DS}	650	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	34	mΩ
I_D	85	A

TO-247



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSU040N65HS	TO-247	040N65H	30pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		650	V
V_{GS}	Gate-Source voltage		±30	V
I_S	Diode continuous forward current	T_C = 25°C	85	A
I_D	Continuous drain current @VGS=10V	T_C = 25°C	85	A
I_D	Continuous drain current @VGS=10V	T_C = 100°C	54	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	223	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	6.2	A
		T_A = 70°C	4.9	A
EAS	Avalanche energy, single pulsed ②		1280	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	625	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	3.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.17	0.20	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	32	38	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=650V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)⑦	V_{DS}=520V,V_{GS}=0V	--	--	50	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.9	3.4	3.9	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=30A	--	34	40	mΩ
		Tj=100℃ ⑦	--	51	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=400V,V_{GS}=0V, f=100kHz	--	6315	--	pF
Coss	Output Capacitance ⑦		--	100	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	5	--	pF
Rg	Gate Resistance ⑦	f=1MHz	--	1.2	--	Ω
Qg	Total Gate Charge ⑦	V_{DS}=400V,I_D=30A, V_{GS}=10V	--	132	--	nC
Qgs	Gate-Source Charge ⑦		--	34	--	nC
Qgd	Gate-Drain Charge ⑦		--	46	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=400V, I_D=30A, R_G=10Ω, V_{GS}=10V	--	47	--	ns
Tr	Turn-on Rise Time		--	69	--	ns
Td(off)	Turn-Off Delay Time		--	187	--	ns
Tf	Turn-Off Fall Time		--	40	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=30A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time ⑦	Isd=30A, V_{GS}=0V di/dt=100A/μs	--	394	--	ns
Qrr	Reverse Recovery Charge ⑦		--	8.3	--	uC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② EAS of 1280mJ is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 16A, V_{GS} =10V；100% FT tested at L = 10mH, I_{AS} = 8A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad).

⑥ The value of RθJA is measured with the device in a still air environment with TA =25° C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

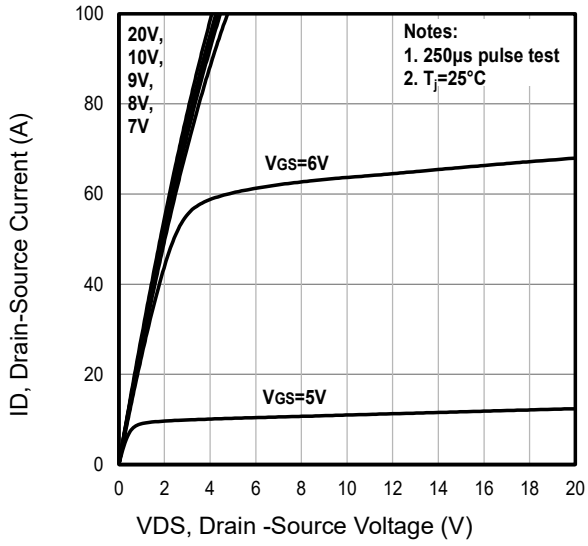


Fig1. Typical Output Characteristics

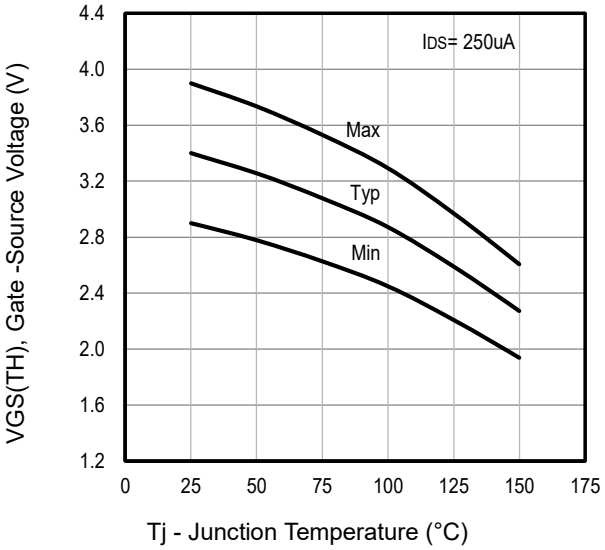


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

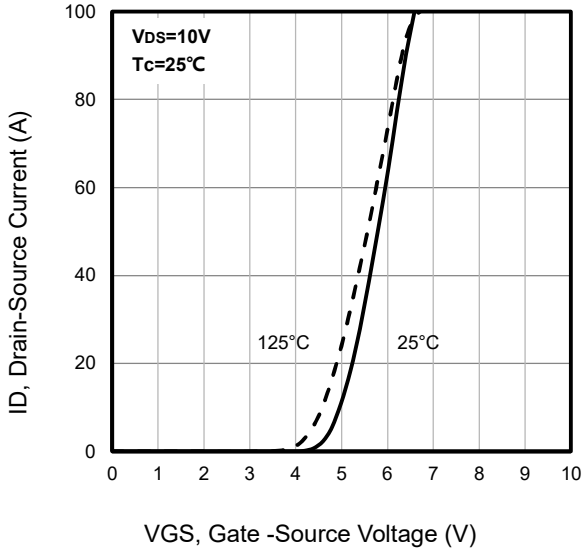


Fig3. Typical Transfer Characteristics

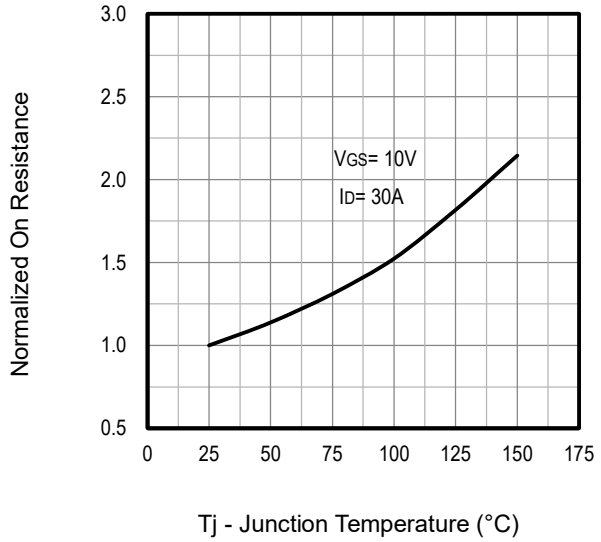


Fig4. Typical Normalized On-Resistance Vs. Tj

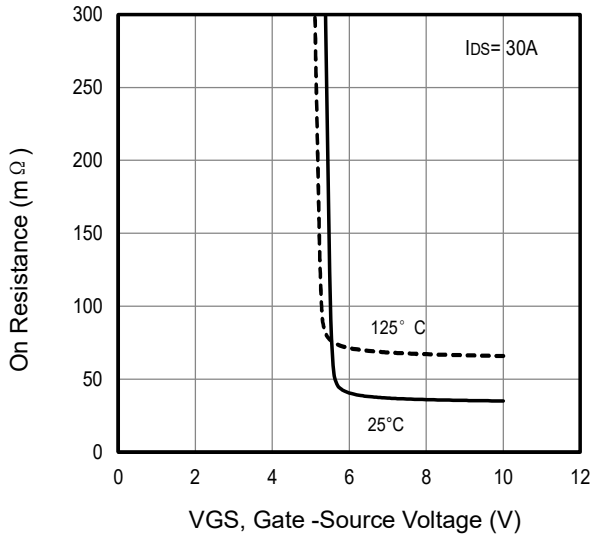


Fig5. Typical On Resistance Vs Gate -Source Voltage

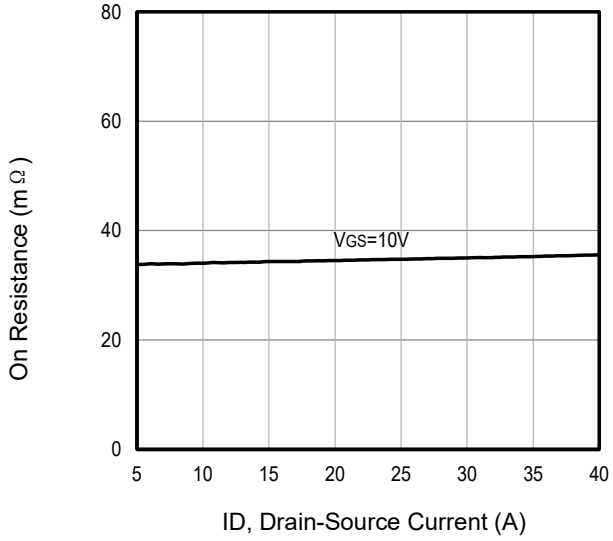


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

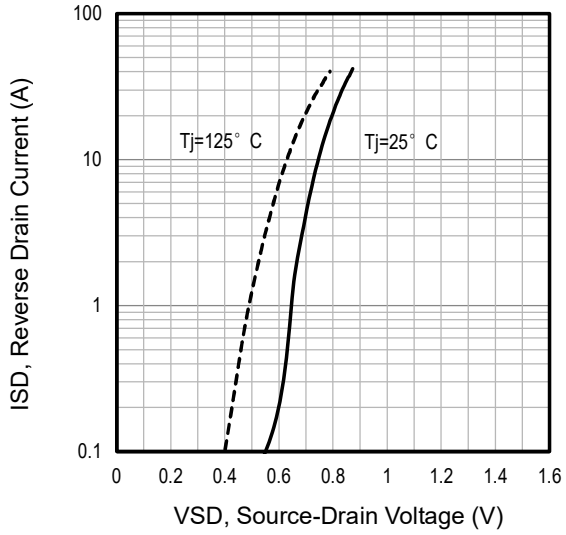


Fig7. Typical Source-Drain Diode Forward Voltage

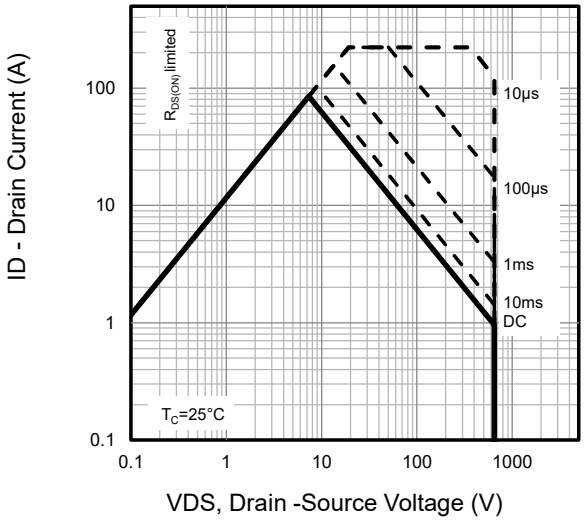


Fig8. Maximum Safe Operating Area

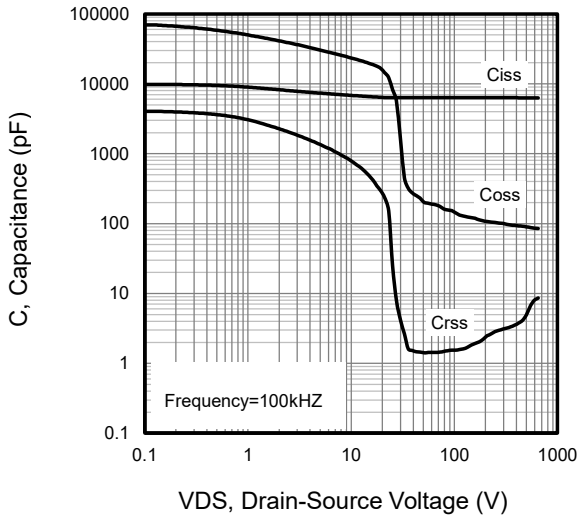


Fig9. Typical Capacitance Vs. Drain-Source Voltage

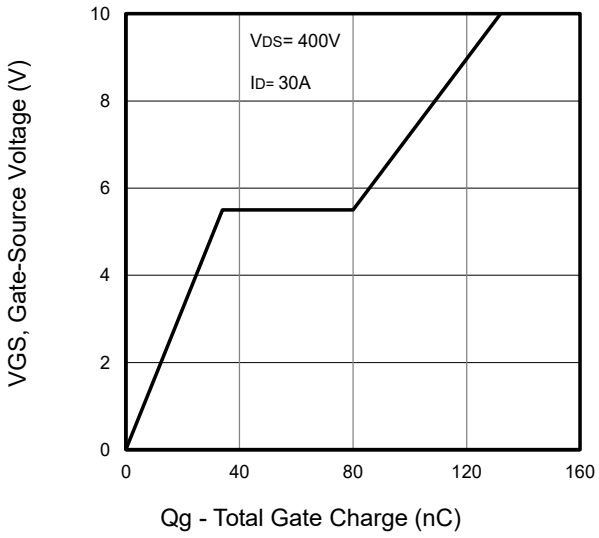


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

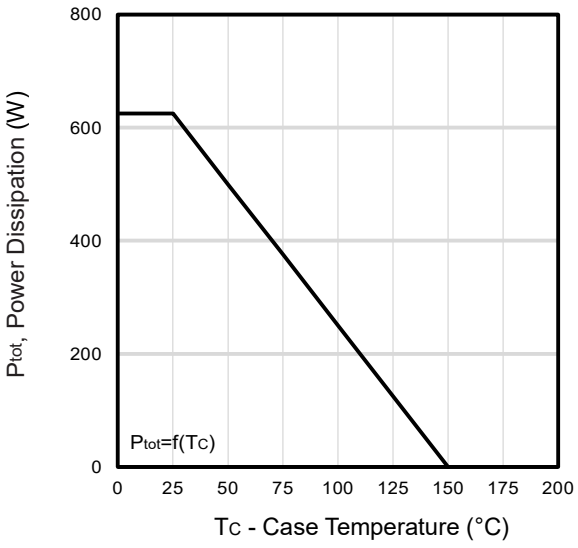


Fig11. Power Dissipation Vs. Case Temperature

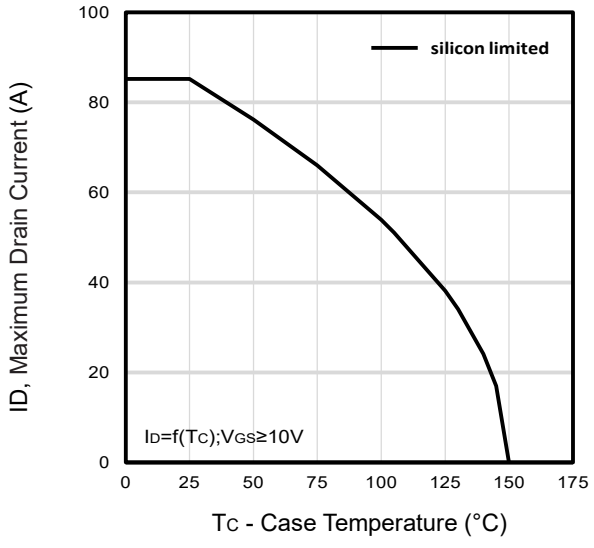


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

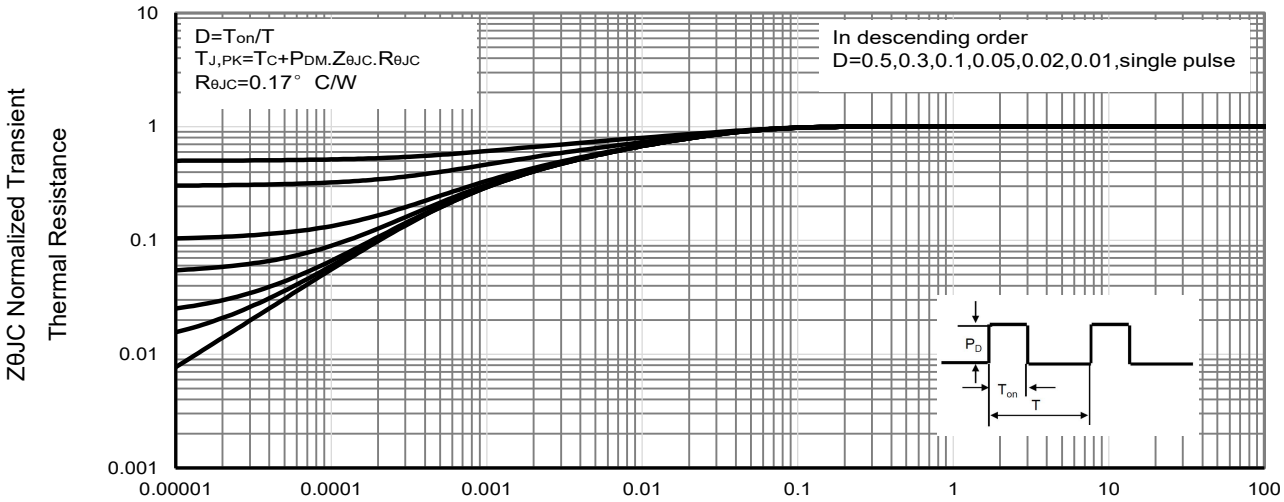


Fig13 . Normalized Maximum Transient Thermal Impedance

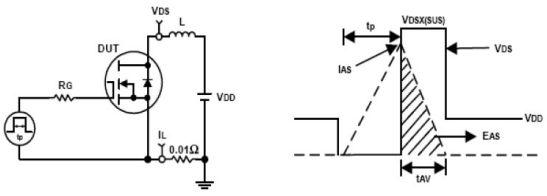


Fig14. Unclamped Inductive Test Circuit and waveforms

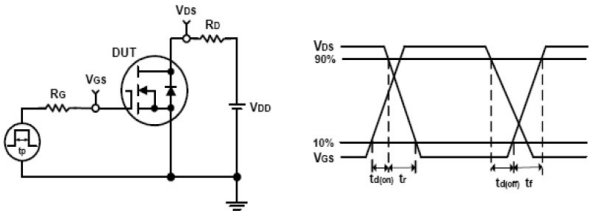
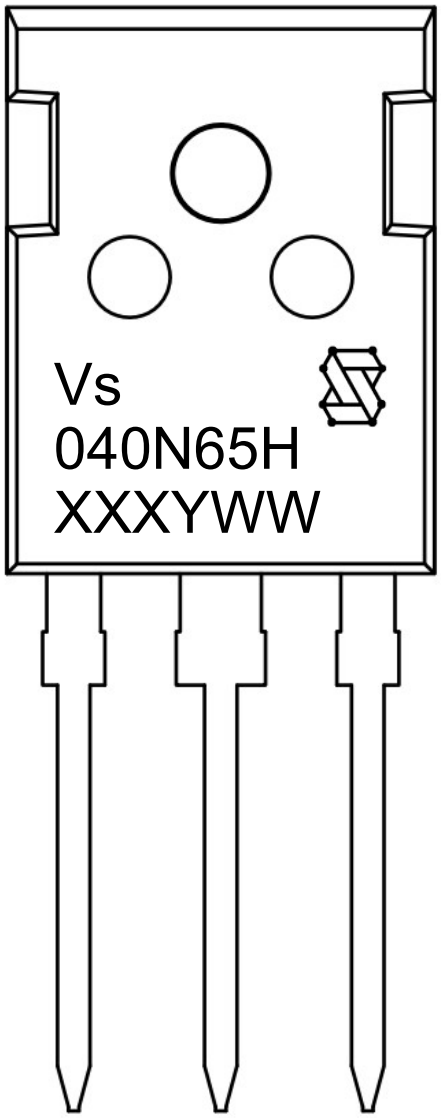


Fig15. Switching Time Test Circuit and waveforms

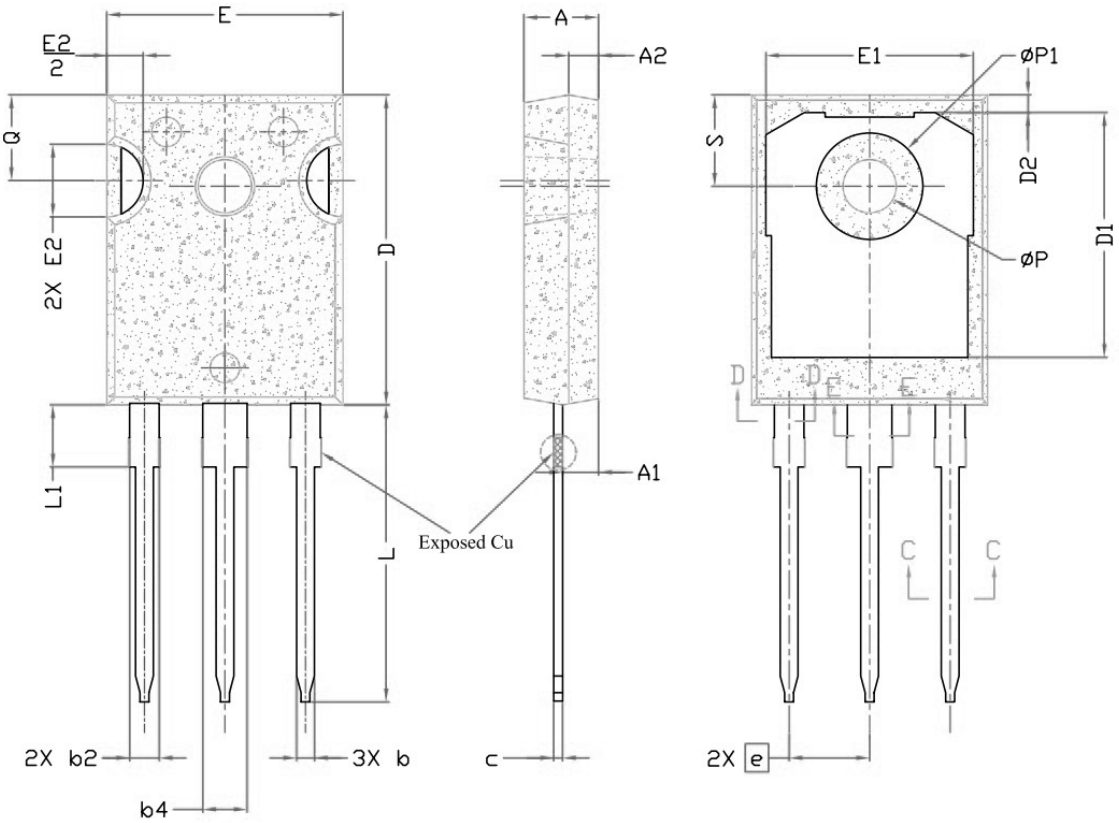
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（040N65H）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.83	5.02	5.21
A1	2.29	2.41	2.55
A2	1.50	2.00	2.49
b	1.12	1.20	1.33
b2	1.91	2.00	2.39
b4	2.87	3.00	3.22
c	0.55	0.60	0.69
D	20.80	20.95	21.10
D1	16.25	16.55	17.65
D2	0.51	1.19	1.35
E	15.7	15.94	16.13
E1	13.1	14.02	14.16
E2	4.32	4.91	5.49
e	5.44 BSC		
L	19.8	20.07	20.32
L1	4.10	4.19	4.40
ΦP	3.56	3.61	3.65
ΦP1	7.19REF.		
Q	5.39	5.79	6.20
S	6.04	6.17	6.30

Notes:

1. Refer to JEDEC TO-247 variation AD
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

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