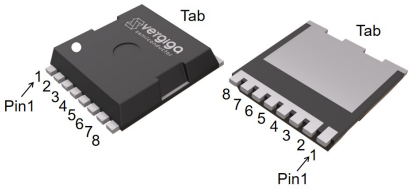
Features

V_{DS}	150	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	9.2	mΩ
$I_{D(Silicon\ Limited)}$	100	A

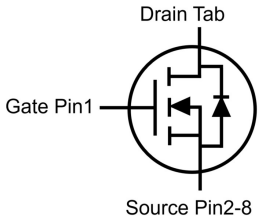
- Enhancement mode
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TOLL



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VSK009N15HS-G	TOLL	009N15H	2000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		150	V
V_{GS}	Gate-Source voltage		±25	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	100	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	100	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	71	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	324	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	11	A
		T_A=70°C	9	A
EAS	Avalanche energy, single pulsed ②		506	mJ
P_D	Maximum power dissipation ③	T_C =25°C	250	W
P_{DSM}	Maximum power dissipation ④	T_A=25°C	2.9	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.5	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	36	43	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	150	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=150V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)⑦	V_{DS}=150V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.6	3.1	3.6	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=40A	--	9.2	12	mΩ
		(Tj=100℃) ⑦	--	12	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=75V,V_{GS}=0V, f=1MHz	2130	4265	7460	pF
Coss	Output Capacitance ⑦		170	340	590	pF
Crss	Reverse Transfer Capacitance ⑦		5	10	30	pF
Rg	Gate Resistance	f=1MHz	0.2	1.5	5	Ω
Qg	Total Gate Charge ⑦	V_{DS}=75V,I_D=40A, V_{GS}=10V	--	55	96	nC
Qgs	Gate-Source Charge ⑦		--	20	35	nC
Qgd	Gate-Drain Charge ⑦		--	9.5	17	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=75V, I_D=40A, R_G=3.9Ω, V_{GS}=10V	--	17	--	ns
Tr	Turn-on Rise Time		--	32	--	ns
Td(off)	Turn-Off Delay Time		--	34	--	ns
Tf	Turn-Off Fall Time		--	20	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time ⑦	I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	--	101	202	ns
Qrr	Reverse Recovery Charge ⑦		--	343	686	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② EAS of 506mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 45A, V_{GS} =10V；100% FT tested at L = 0.5mH, I_{AS} = 23A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

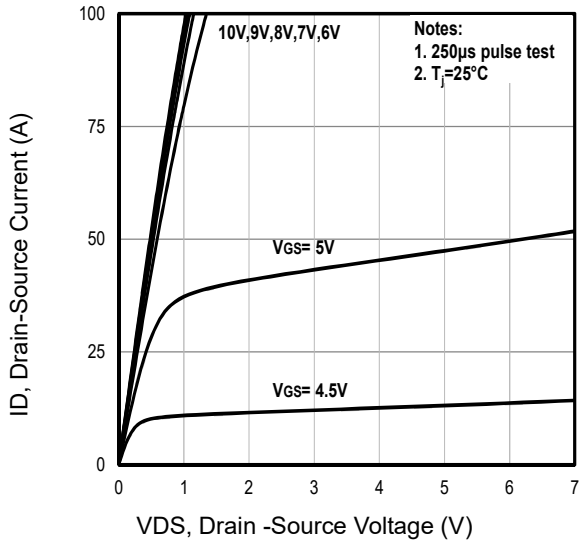


Fig1. Typical Output Characteristics

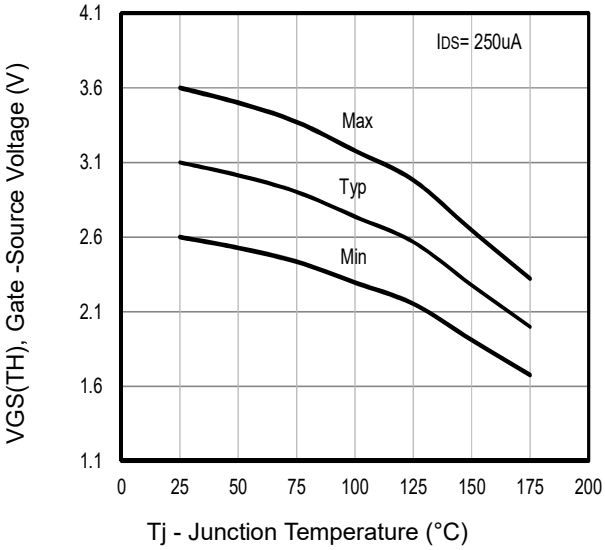


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

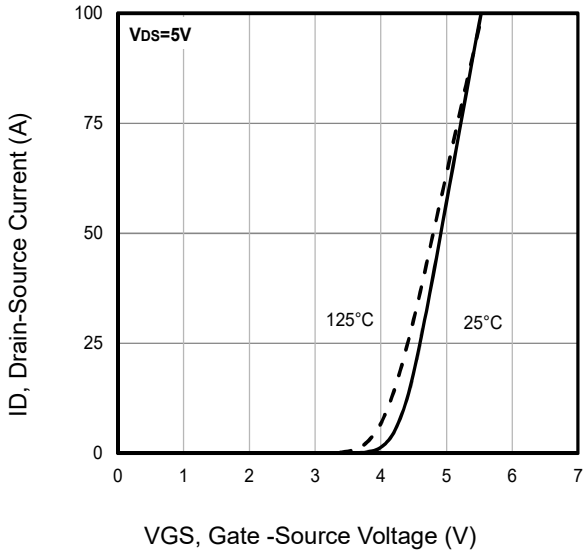


Fig3. Typical Transfer Characteristics

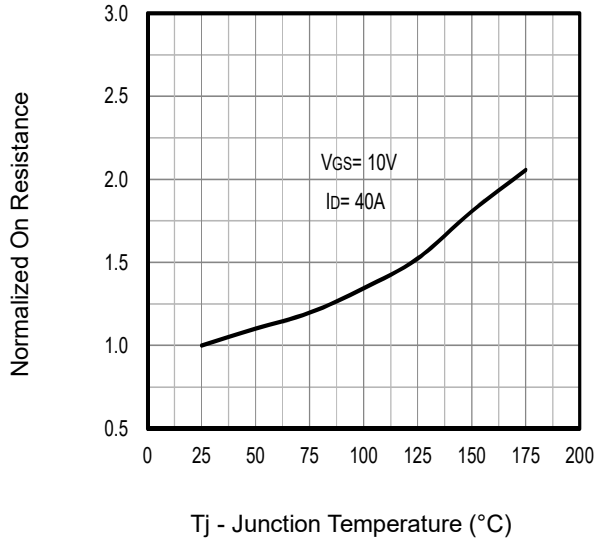


Fig4. Typical Normalized On-Resistance Vs. Tj

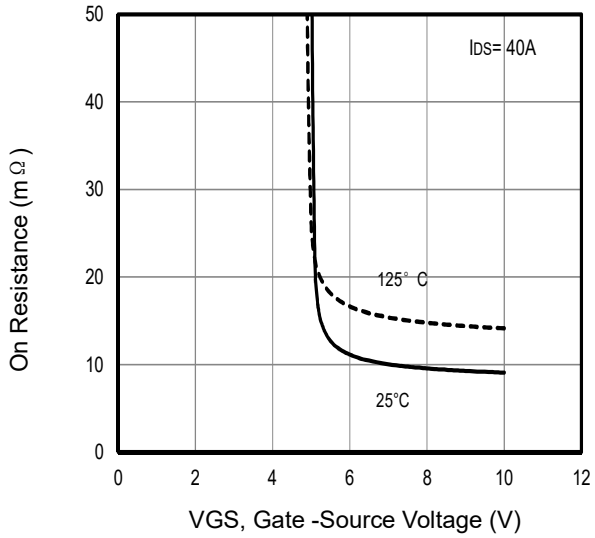


Fig5. Typical On Resistance Vs Gate -Source Voltage

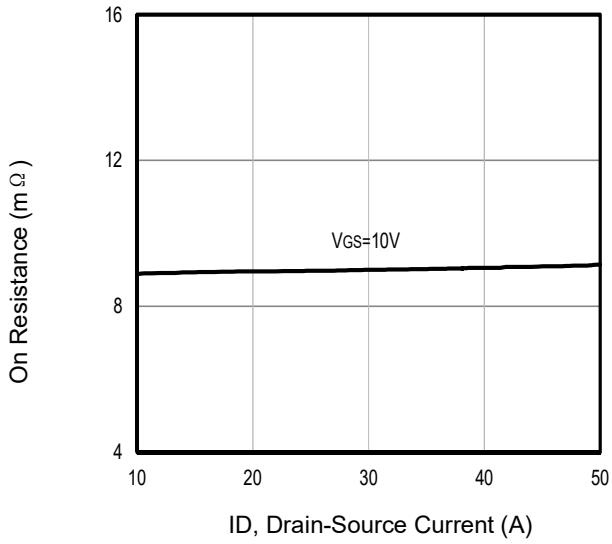


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

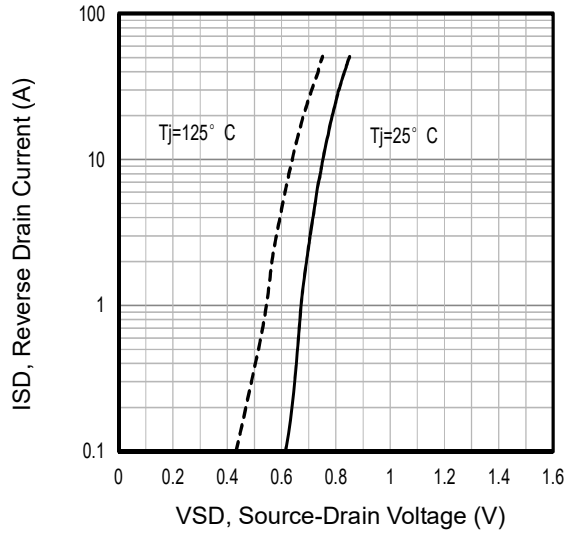


Fig7. Typical Source-Drain Diode Forward Voltage

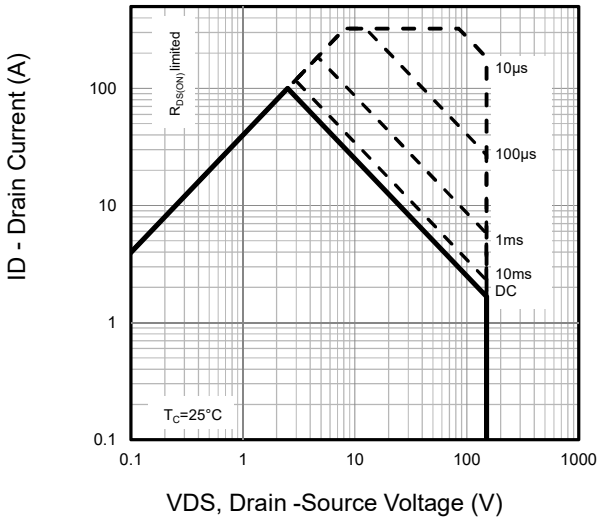


Fig8. Maximum Safe Operating Area

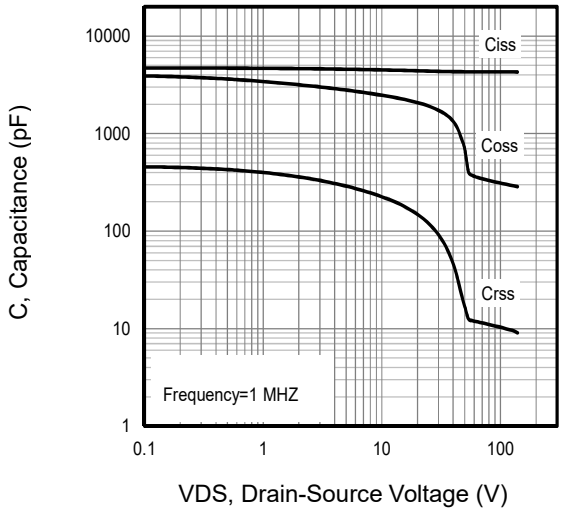


Fig9. Typical Capacitance Vs. Drain-Source Voltage

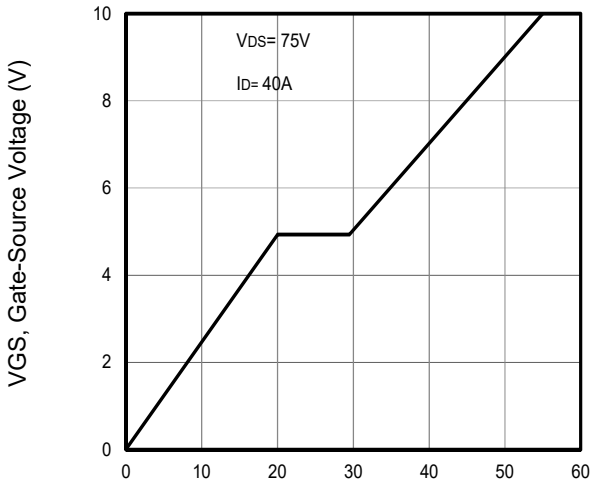


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

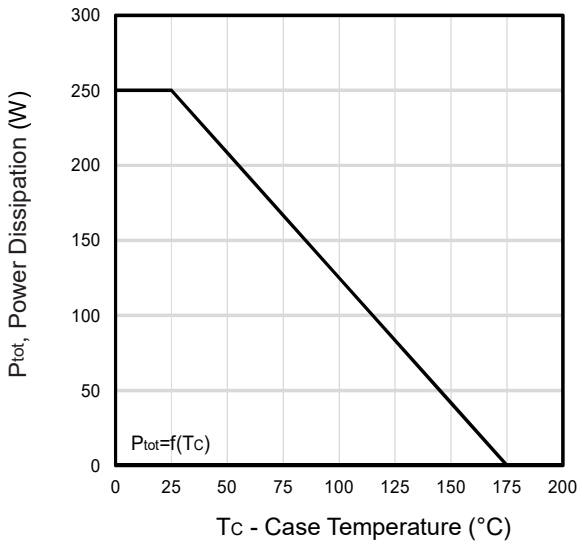


Fig11. Power Dissipation Vs. Case Temperature

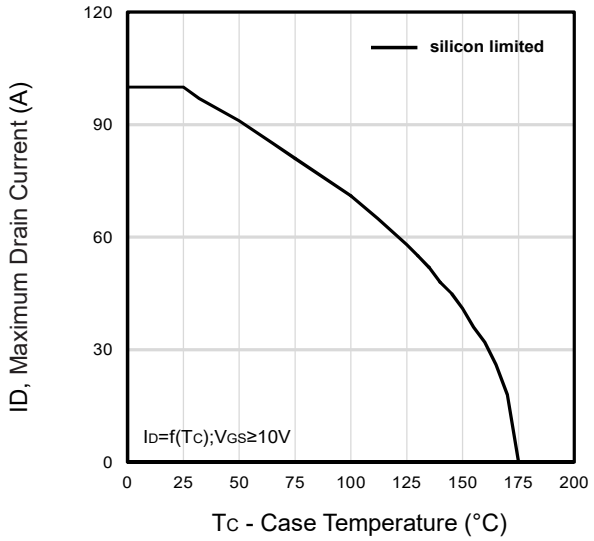


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

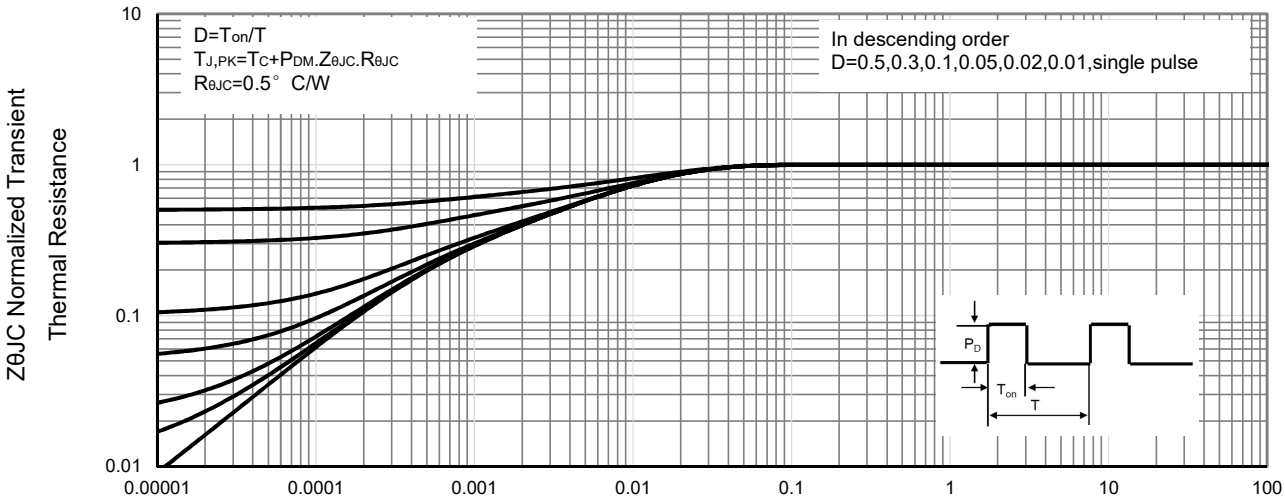


Fig13 . Normalized Maximum Transient Thermal Impedance

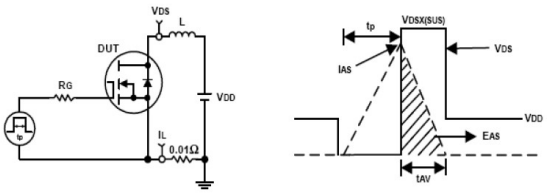


Fig14. Unclamped Inductive Test Circuit and waveforms

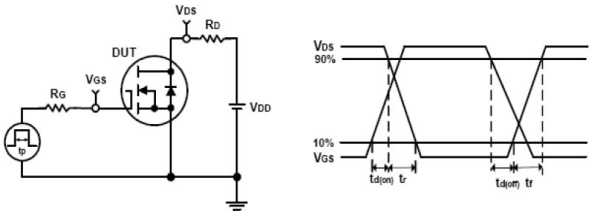
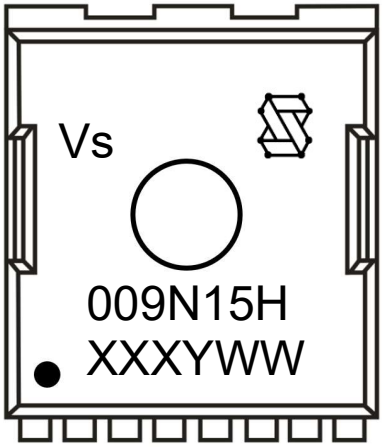


Fig15. Switching Time Test Circuit and waveforms

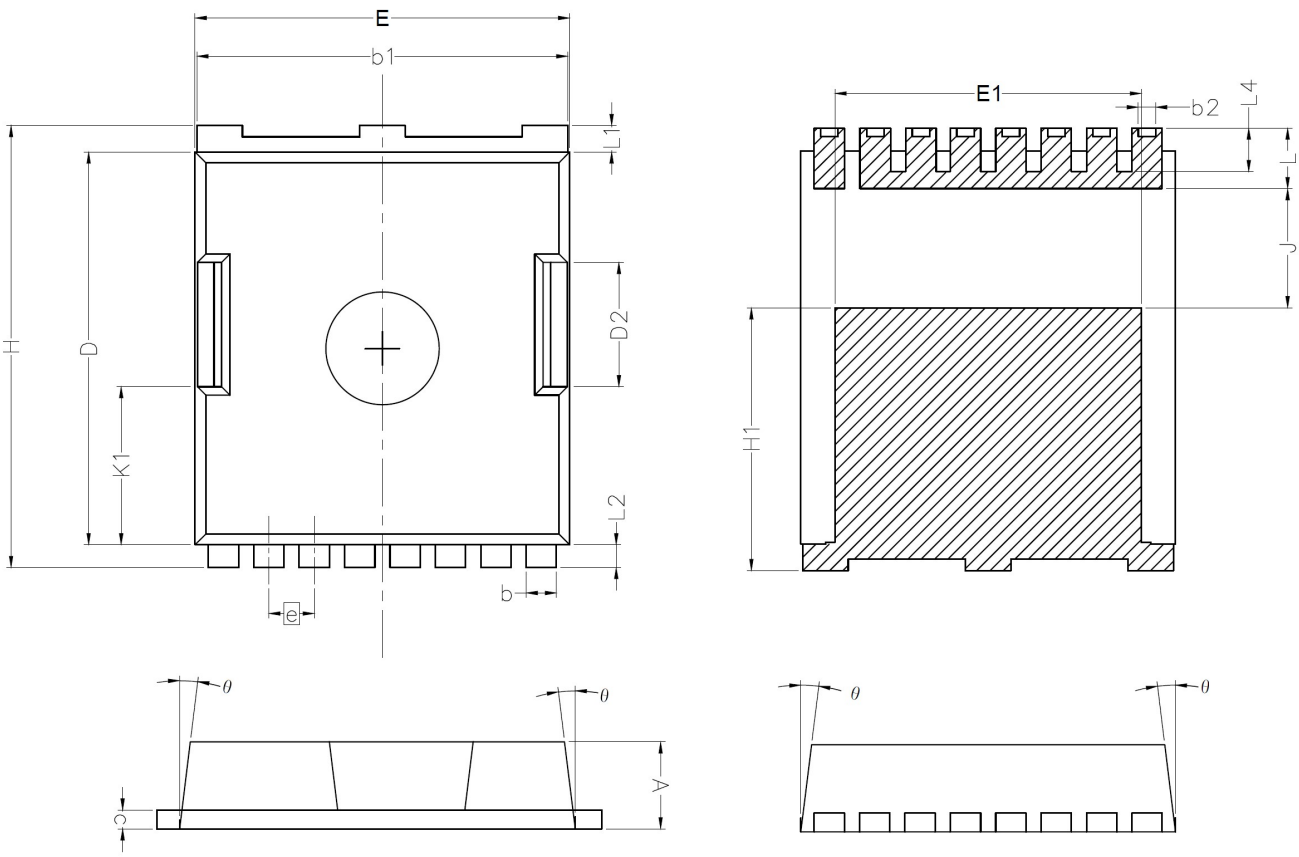
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（009N15H）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TOLL Package Outline Data



Note:

1. All dimensions are in mm,angles in degrees.
2. Dimensions do not include mold flash protrusions or gate burrs.

Symbol	DIMENSIONS (unit : mm)			Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max		Min	Typ	Max
A	2.20	--	2.40	H	11.48	11.68	11.88
b	0.70	--	0.90	H1	6.75	6.95	7.15
b1	9.70	--	9.90	N	--	8	--
b2	0.42	--	0.50	J	3.00	3.15	3.30
c	0.40	--	0.60	K1	3.98	4.18	4.38
D	10.28	--	10.58	L	1.40	1.60	1.80
D2	3.10	3.30	3.50	L1	0.60	0.70	0.80
E	9.70	9.90	10.10	L2	0.50	0.60	0.70
E1	7.90	8.10	8.30	L4	1.00	1.15	1.30
e	1.20BSC			θ	4°	7°	10°

Customer Service

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WEB: **www.vergiga.com**