

Features

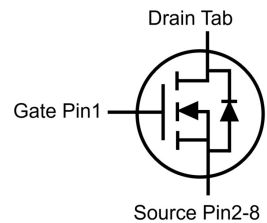
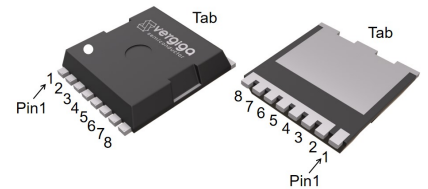
- Enhancement mode
- Very Low on-resistance $R_{DS(on)}$
- VitoMOS[®] II Technology
- Fast Switching and High efficiency
- 100% Avalanche test


Halogen-Free

Part ID	Package Type	Marking	Packing
VSK002N08HC-G	TOLL	002N08H	2000PCS/Reel

V_{DS}	80	V
$R_{DS(on),TYP@ V_{GS}=10V}$	1.3	mΩ
I_D (Silicon Limited)	300	A
I_D (Package Limited)	255	A

TOLL



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	80	V	
V_{GS}	Gate-Source voltage	±25	V	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	300	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$	300	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$	212	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	255	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	1200	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	32	A
		$T_A = 70^\circ\text{C}$	25	A
E_{AS}	Avalanche energy, single pulsed ②	400	mJ	
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	283	W
		$T_C = 100^\circ\text{C}$	142	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 70^\circ\text{C}$	2	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	°C	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.53	0.64	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	48	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	80	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _J =25°C)	V _{DS} =80V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =80V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.3	2.8	3.3	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =80A	--	1.3	1.7	mΩ
		(T _J =100°C)	--	1.6	--	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =40V, V _{GS} =0V, f=1MHz	6155	12310	21540	pF
C _{oss}	Output Capacitance		1335	2670	4675	pF
C _{rss}	Reverse Transfer Capacitance		20	45	80	pF
R _g	Gate Resistance	f=1MHz	0.2	0.7	5	Ω
Q _g	Total Gate Charge	V _{DS} =40V, I _D =80A, V _{GS} =10V	--	204	357	nC
Q _{gs}	Gate-Source Charge		--	47	82	nC
Q _{gd}	Gate-Drain Charge		--	67	117	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =40V, I _D =80A, R _G =3Ω, V _{GS} =10V	--	28	--	ns
T _r	Turn-on Rise Time		--	102	--	ns
T _{d(off)}	Turn-Off Delay Time		--	88	--	ns
T _f	Turn-Off Fall Time		--	58	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =80A, V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time	T _J =25°C, I _{sd} =80A, V _{GS} =0V	--	120	240	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	183	366	nC

NOTE: ① Single pulse; pulse width ≤ 100μs.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 40A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

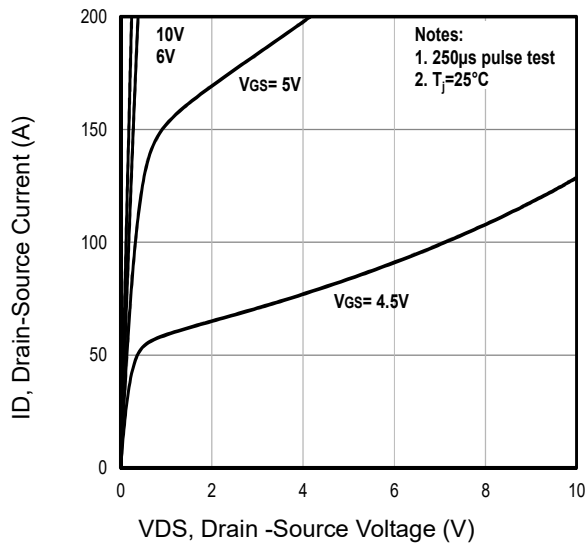


Fig1. Typical Output Characteristics

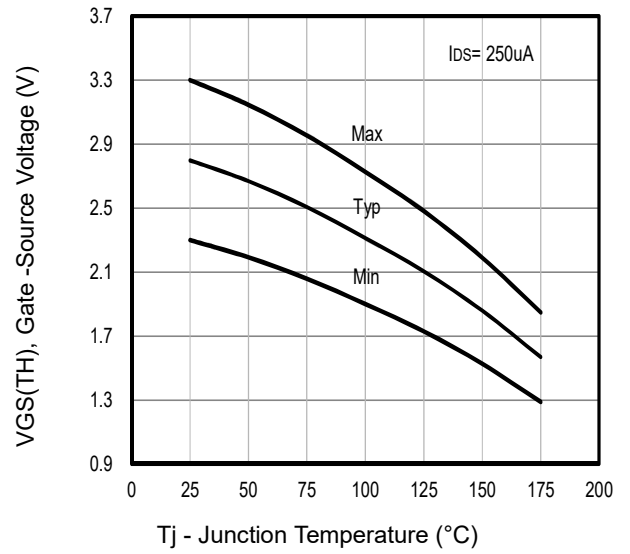


Fig2. Typical V_{GS(TH)} Gate-Source Voltage Vs. T_j

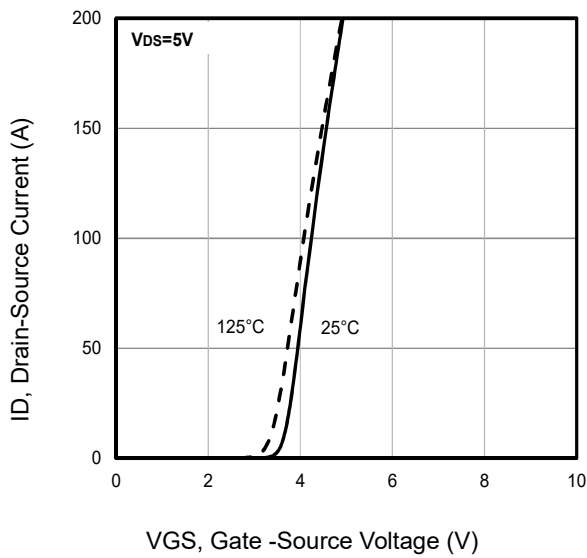


Fig3. Typical Transfer Characteristics

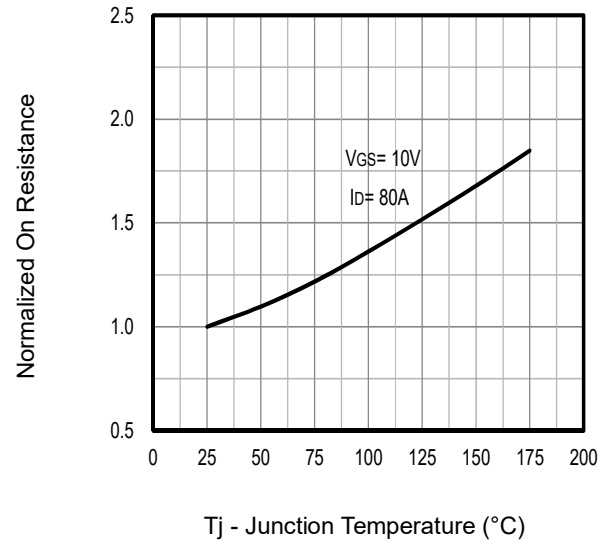


Fig4. Typical Normalized On-Resistance Vs. T_j

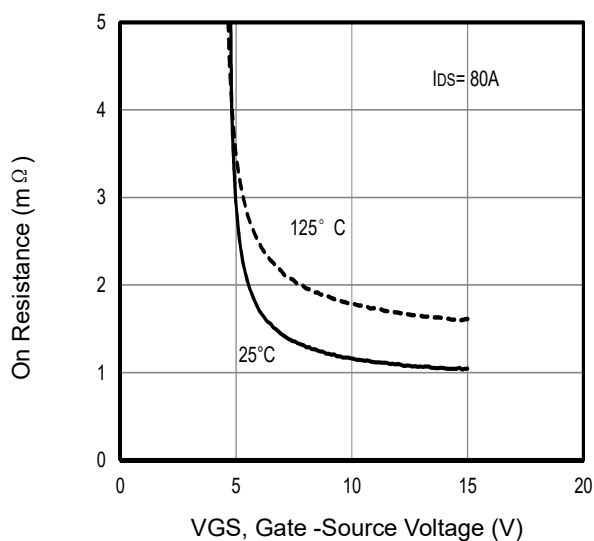


Fig5. Typical On Resistance Vs Gate-Source Voltage

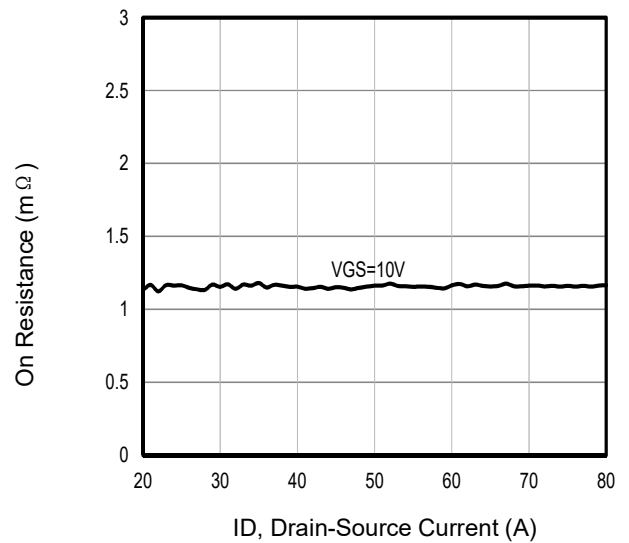


Fig6. Typical On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

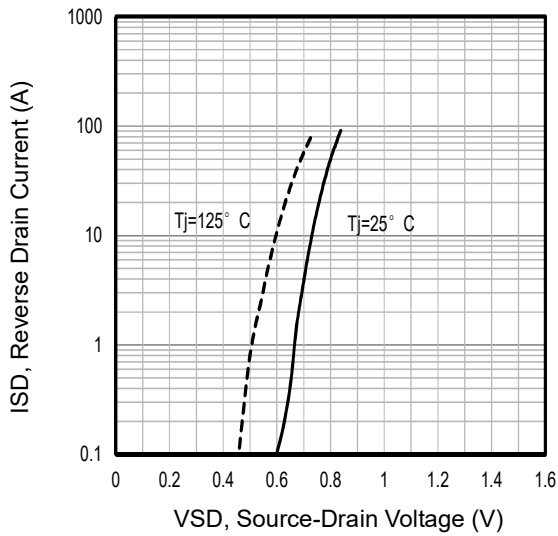


Fig7. Typical Source-Drain Diode Forward Voltage

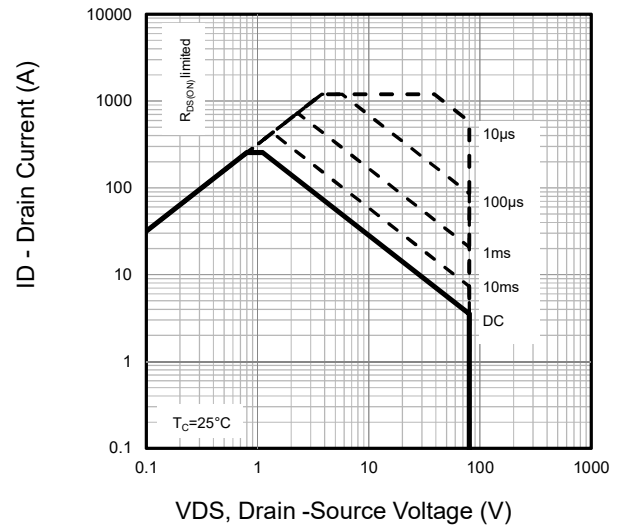


Fig8. Maximum Safe Operating Area

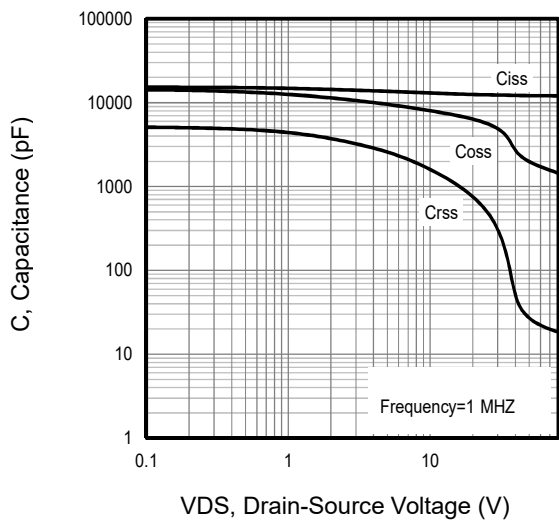


Fig9. Typical Capacitance Vs. Drain-Source Voltage

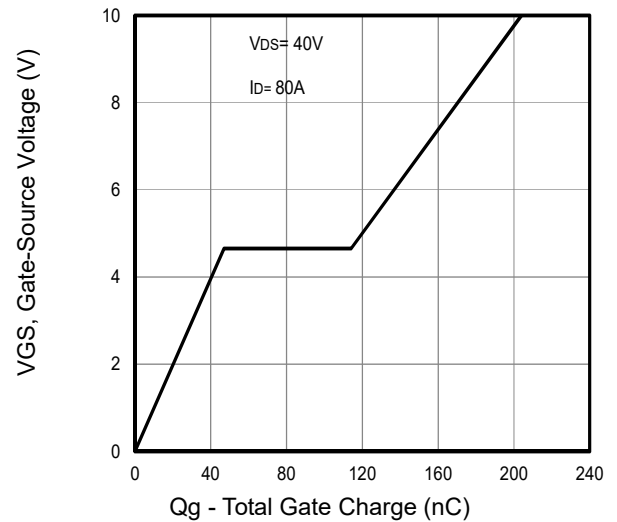


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

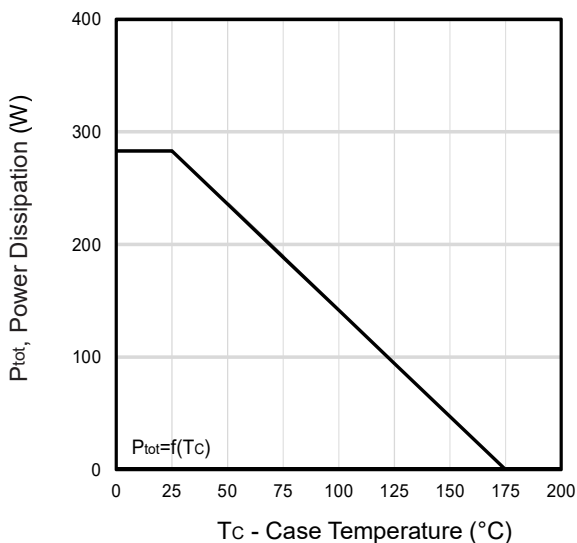


Fig11. Power Dissipation Vs. Case Temperature

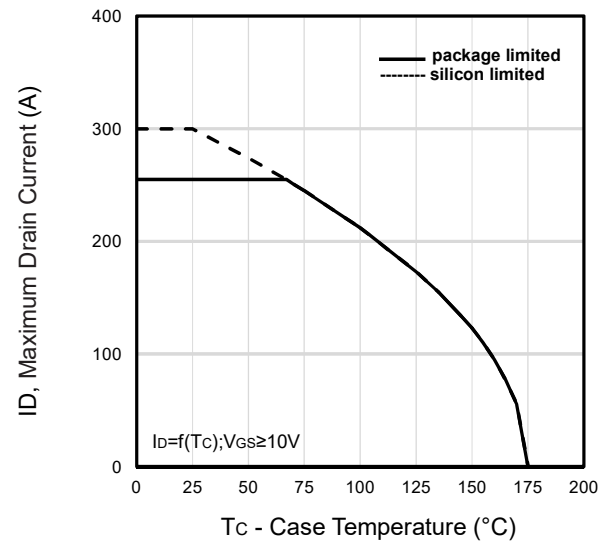


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

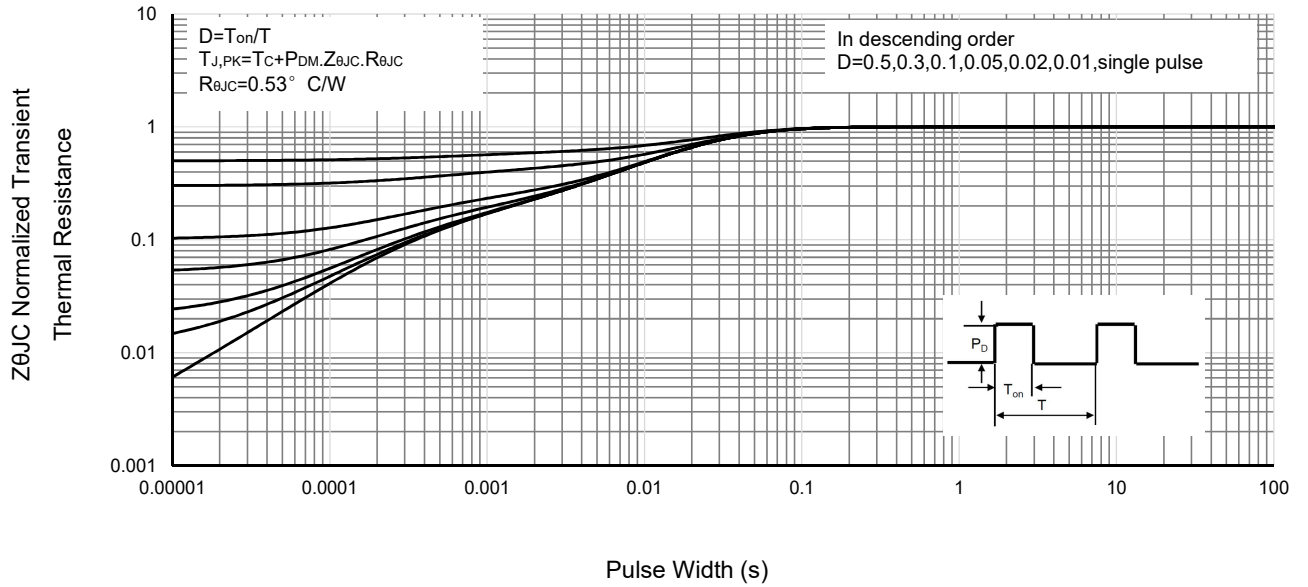


Fig13 . Normalized Maximum Transient Thermal Impedance

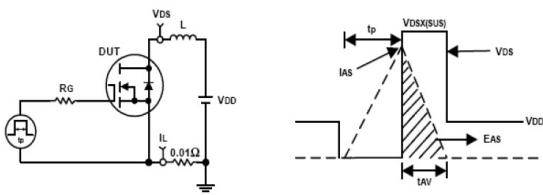


Fig14. Unclamped Inductive Test Circuit and waveforms

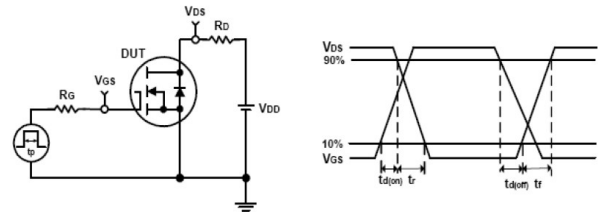
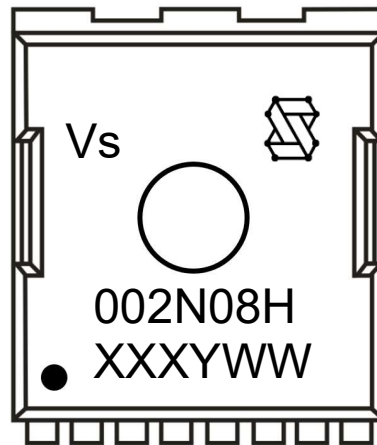


Fig15. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (002N08H)

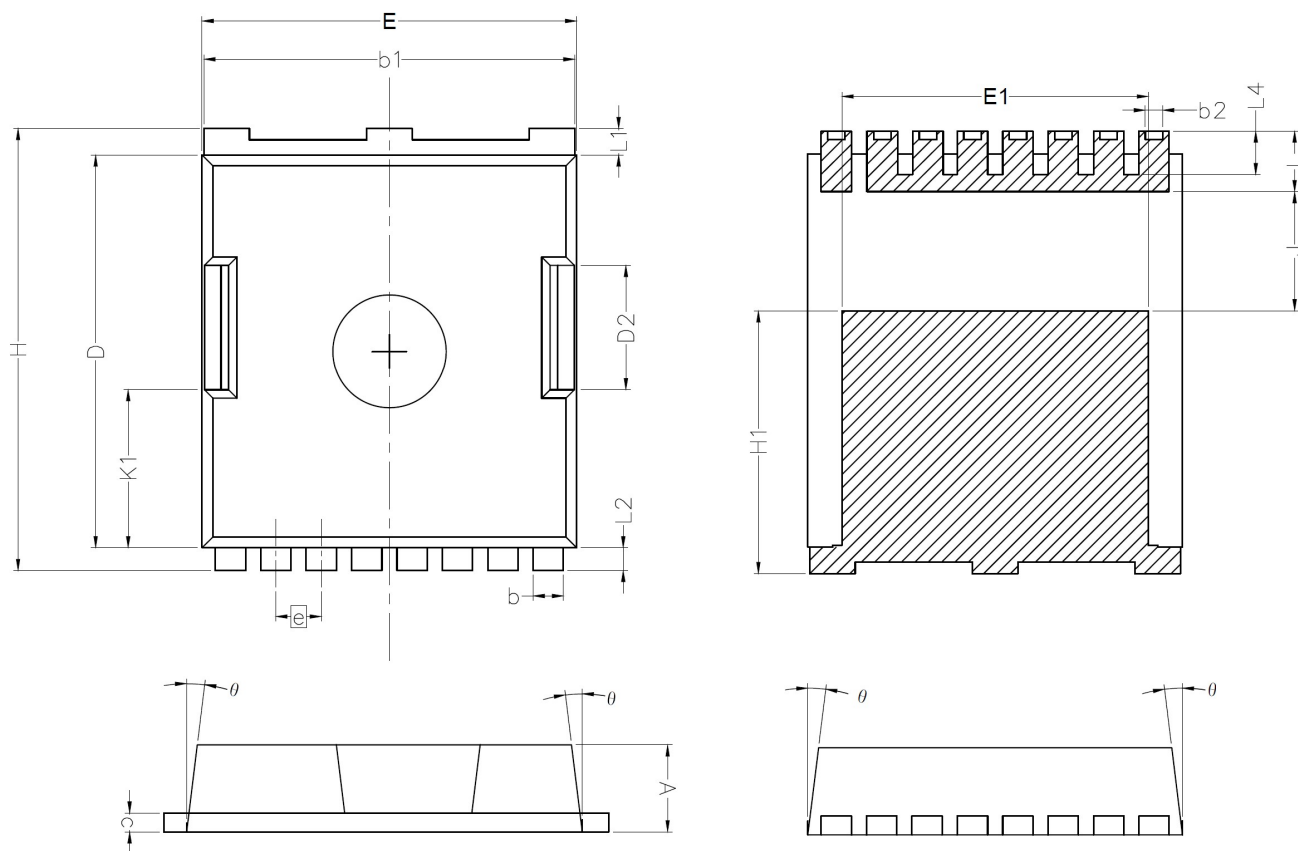
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TOLL Package Outline Data

Note:

1. All dimensions are in mm, angles in degrees.
2. Dimensions do not include mold flash protrusions or gate burrs.

Symbol	DIMENSIONS (unit : mm)			Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max		Min	Typ	Max
A	2.20	--	2.40	H	11.48	11.68	11.88
b	0.70	--	0.90	H1	6.75	6.95	7.15
b1	9.70	--	9.90	N	--	8	--
b2	0.42	--	0.50	J	3.00	3.15	3.30
c	0.40	--	0.60	K1	3.98	4.18	4.38
D	10.28	--	10.58	L	1.40	1.60	1.80
D2	3.10	3.30	3.50	L1	0.60	0.70	0.80
E	9.70	9.90	10.10	L2	0.50	0.60	0.70
E1	7.90	8.10	8.30	L4	1.00	1.15	1.30
e	1.20BSC			θ	4°	7°	10°

Customer Service
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