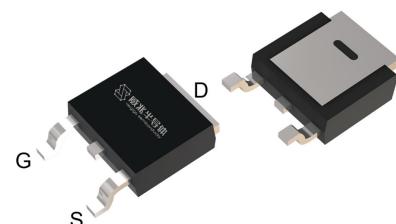


Features

- Enhancement mode
- Very low on-resistance $R_{DS(on)}$
- VitoMOS® II Technology
- Fast Switching and High efficiency
- 100% Avalanche test

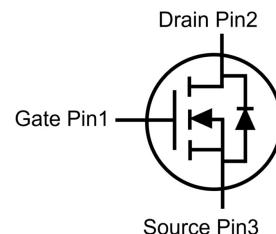
V_{DS}	40	V
$R_{DS(on),TYP}@ V_{GS}=10V$	3.6	$m\Omega$
$R_{DS(on),TYP}@ V_{GS}=4.5V$	5.3	$m\Omega$
I_D	90	A

TO-252



Halogen-Free

Part ID	Package Type	Marking	Packing
VSD007N04MS-G	TO-252	007N04M	2500PCS/Reel



Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V(BR)DSS$	Drain-Source breakdown voltage	40	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ C$	A
I_D	Continuous drain current @ $V_{GS}=10V$	$T_C = 25^\circ C$	A
		$T_C = 100^\circ C$	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ C$	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ C$	A
		$T_A = 70^\circ C$	A
E_{AS}	Avalanche energy, single pulsed ②	45	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ C$	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ C$	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.95	3.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	120	$^\circ C/W$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	--	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=125^\circ\text{C}$)	$V_{DS}=40\text{V}, V_{GS}=0\text{V}$	--	--	100	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.2	1.7	2.3	V
RDS(on)	Drain-Source On-State Resistance ④	$V_{GS}=10\text{V}, I_D=30\text{A}$	--	3.6	4.5	$\text{m}\Omega$
		$T_j=100^\circ\text{C}$	--	4.3	--	$\text{m}\Omega$
RDS(on)	Drain-Source On-State Resistance ④	$V_{GS}=4.5\text{V}, I_D=20\text{A}$	--	5.3	6.6	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
Ciss	Input Capacitance	$V_{DS}=20\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	970	1295	1720	pF
Coss	Output Capacitance		370	490	650	pF
Crss	Reverse Transfer Capacitance		20	30	40	pF
Rg	Gate Resistance	f=1MHz	0.2	1.5	3	Ω
Qg(10V)	Total Gate Charge	$V_{DS}=20\text{V}, I_D=30\text{A}, V_{GS}=10\text{V}$	--	27	36	nC
Qg(4.5V)			--	14	19	nC
Qgs	Gate-Source Charge		--	4.4	5.9	nC
Qgd	Gate-Drain Charge		--	6.1	9.2	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	$V_{DD}=20\text{V}, I_D=30\text{A}, R_G=3\Omega, V_{GS}=10\text{V}$	--	7.2	--	ns
Tr	Turn-on Rise Time		--	61	--	ns
Td(off)	Turn-Off Delay Time		--	24	--	ns
Tf	Turn-Off Fall Time		--	33	--	ns
Source- Drain Diode Characteristics@ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
VSD	Forward on voltage	$I_{SD}=30\text{A}, V_{GS}=0\text{V}$	--	0.9	1.2	V
Trr	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_{SD}=30\text{A}, V_{GS}=0\text{V}$ $dI/dt=100\text{A}/\mu\text{s}$	--	19	38	ns
Qrr	Reverse Recovery Charge		--	6.7	13.5	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 30\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{0JA} and the maximum allowed junction temperature of 150°C .
- ④ Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics

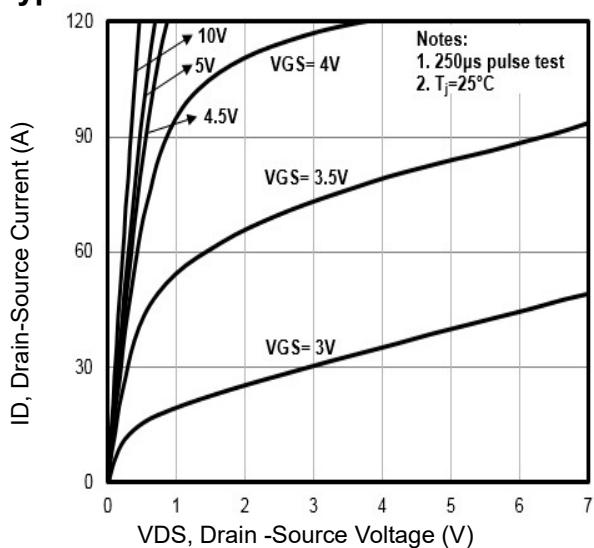


Fig1. Typical Output Characteristics

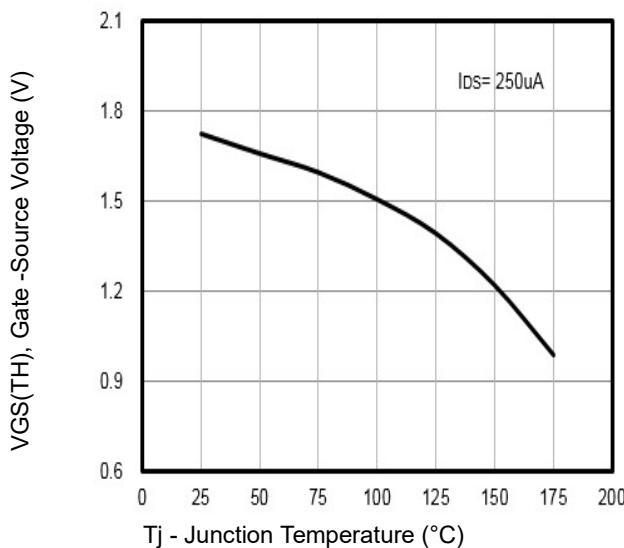


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

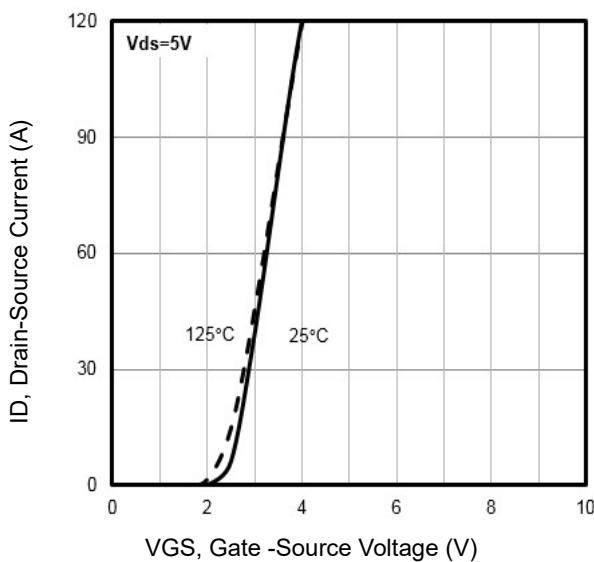


Fig3. Typical Transfer Characteristics

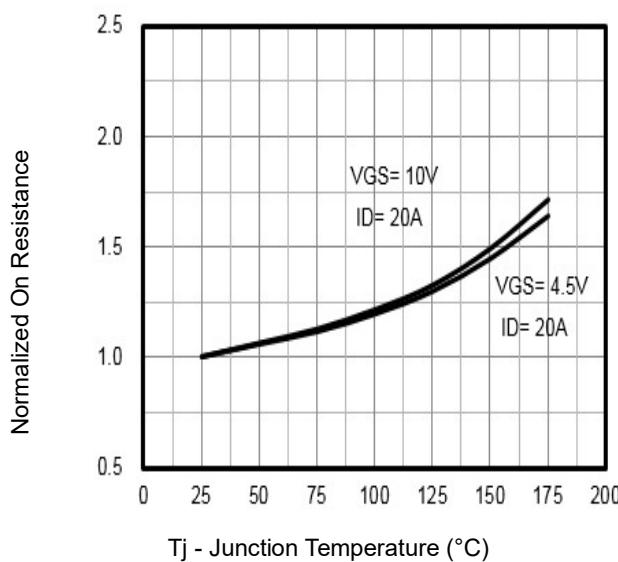


Fig4. Normalized On-Resistance Vs. T_j

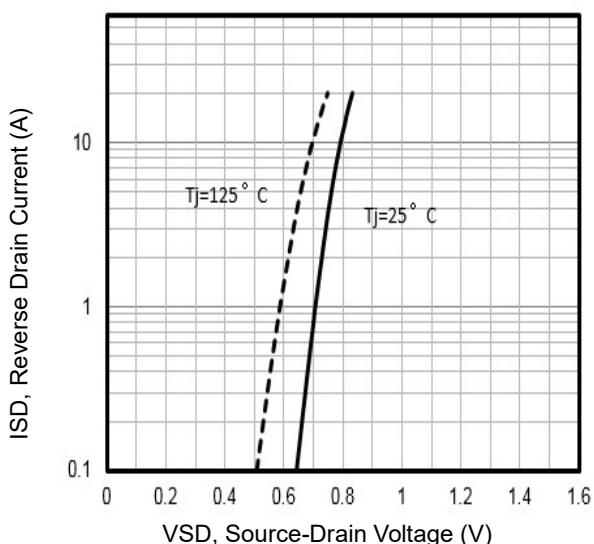


Fig5. Typical Source-Drain Diode Forward Voltage

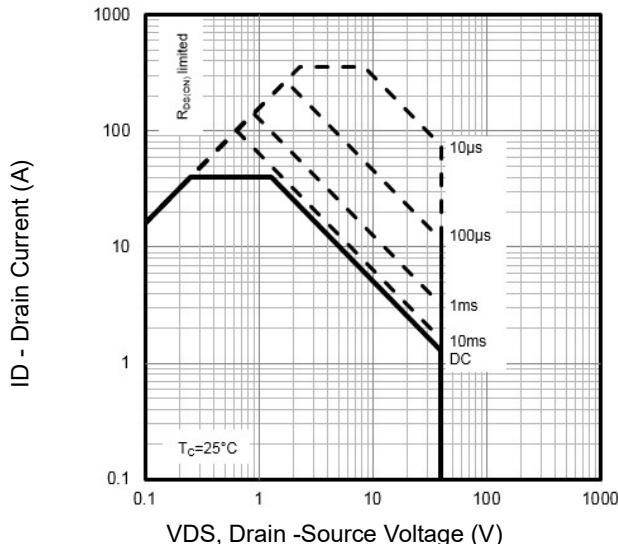


Fig6. Maximum Safe Operating Area

Typical Characteristics

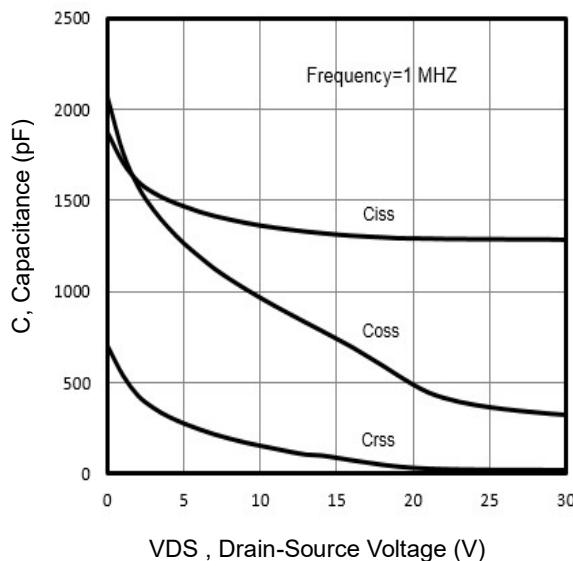


Fig7. Typical Capacitance Vs.Drain-Source Voltage

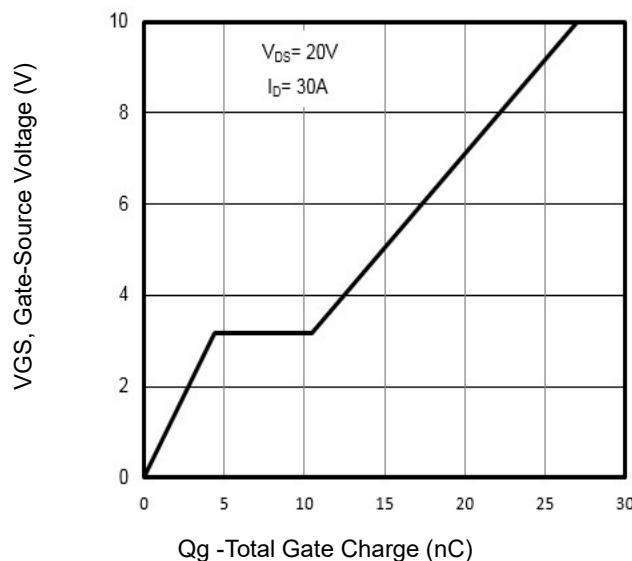


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

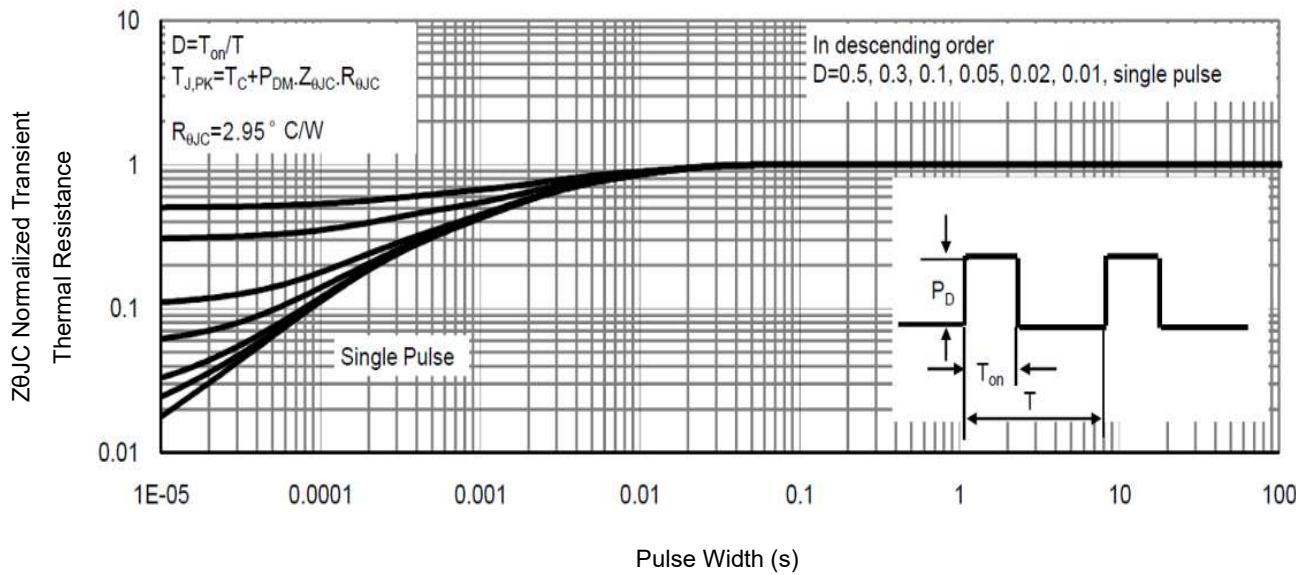


Fig9. Normalized Maximum Transient Thermal Impedance

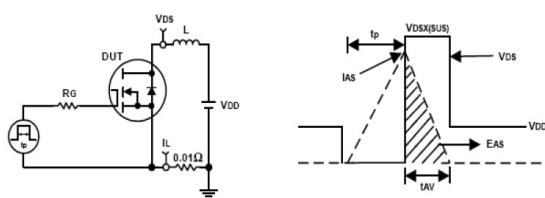


Fig10. Unclamped Inductive Test Circuit and waveforms

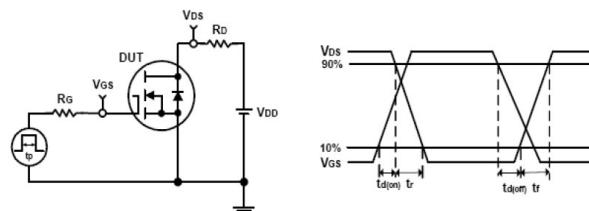
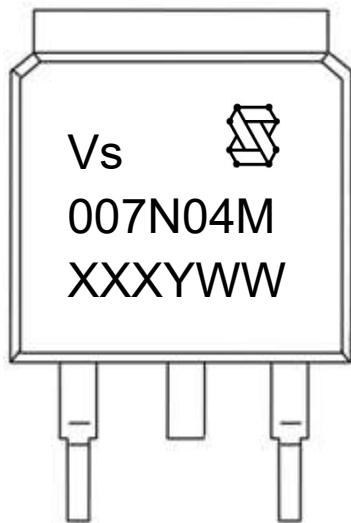


Fig11. Switching Time Test Circuit and waveforms

Marking Information

1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (007N04M)

3rd line: Date code (XXXYWW)

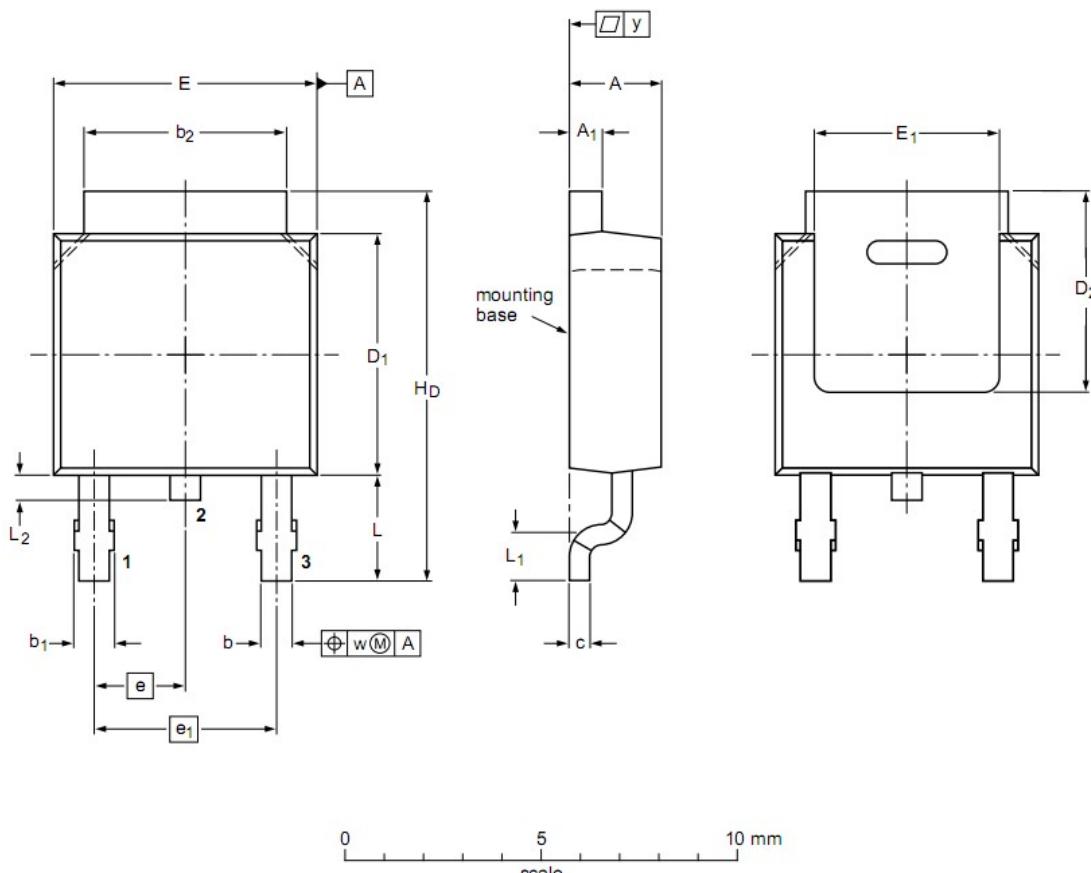
XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b₁	0.77	0.85	1.14
b₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D₁	5.98	6.10	6.223
D₂	5.21	--	--
E	6.40	6.60	6.731
E₁	4.40	--	--
e	2.286 BSC		
e₁	--	4.57	--
H_b	9.40	10.00	10.40
L	2.743 REF		
L₁	1.40	1.52	1.77
L₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

- Refer to JEDEC TO-252 variation AA
- Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
- Dimension "D₁" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

Customer Service

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