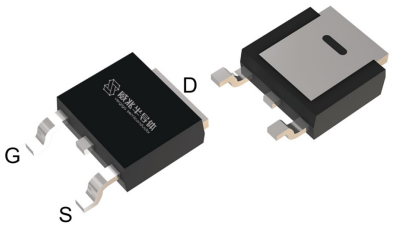
Features

- N-Channel，5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

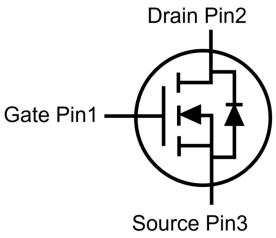
V_{DS}	30	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	3	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	4.4	mΩ
I_D	105	A

TO-252



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VSD005N03MS	TO-252	005N03M	2500PCS/Reel



Maximum ratings, at T_j=25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	V
I_S	Diode continuous forward current	T_C=25°C	105	A
I_D	Continuous drain current @VGS=10V	T_C=25°C	105	A
		T_C=100°C	66	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	420	A
EAS	Avalanche energy, single pulsed ②		81	mJ
P_D	Maximum power dissipation	T_C=25°C	54	W
VGS	Gate-Source voltage		±20	V
T_{STG} T_J	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance- Junction to Case	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance- Junction to Ambient	100	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_C = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=30V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=30V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1	1.8	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=10V, I_D=20A	--	3	4	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=4.5V, I_D=15A	--	4.4	6	mΩ
Dynamic Electrical Characteristics @ T_C= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz	--	2525	--	pF
C_{oss}	Output Capacitance		--	380	--	pF
C_{rss}	Reverse Transfer Capacitance		--	290	--	pF
R_g	Gate Resistance	f=1MHz	--	1.0	--	Ω
Q_g	Total Gate Charge	V_{DS}=15V,I_D=20A, V_{GS}=10V	--	43	--	nC
Q_{gs}	Gate-Source Charge		--	8.6	--	nC
Q_{gd}	Gate-Drain Charge		--	7.8	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V, I_D=20A, R_G=3.0Ω, V_{GS}=10V	--	9	--	ns
t_r	Turn-on Rise Time		--	6	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	42.6	--	ns
t_f	Turn-Off Fall Time		--	11.8	--	ns
Source- Drain Diode Characteristics@ T_C = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=20A, V_{GS}=0V di/dt=500A/μs	--	18.6	--	ns
Q_{rr}	Reverse Recovery Charge		--	32	--	nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} =10V. Part not recommended for use above this value

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

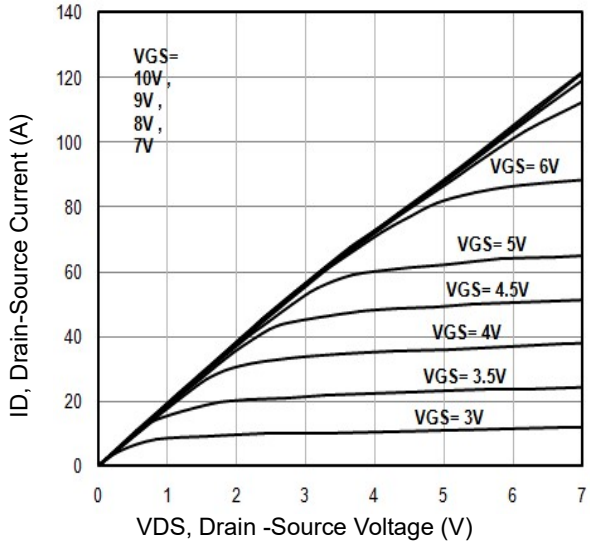


Fig1. Typical Output Characteristics

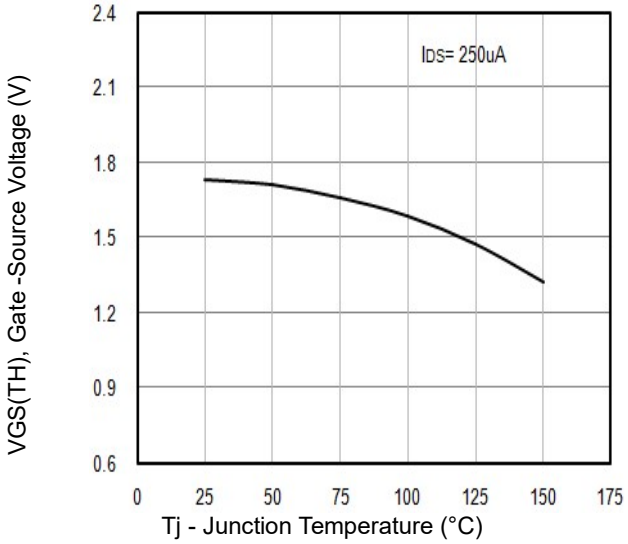


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

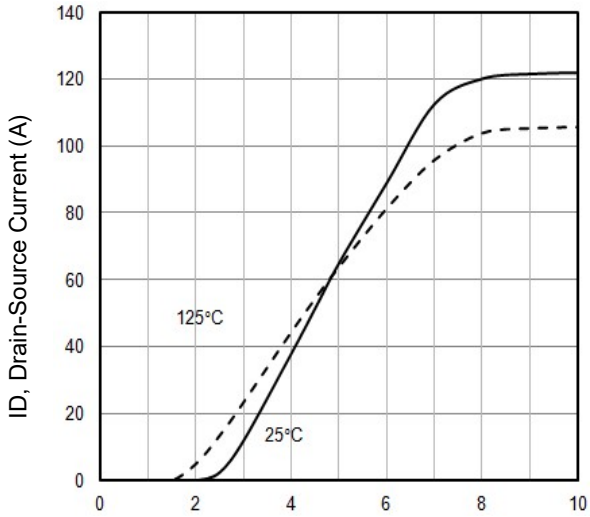


Fig3. Typical Transfer Characteristics

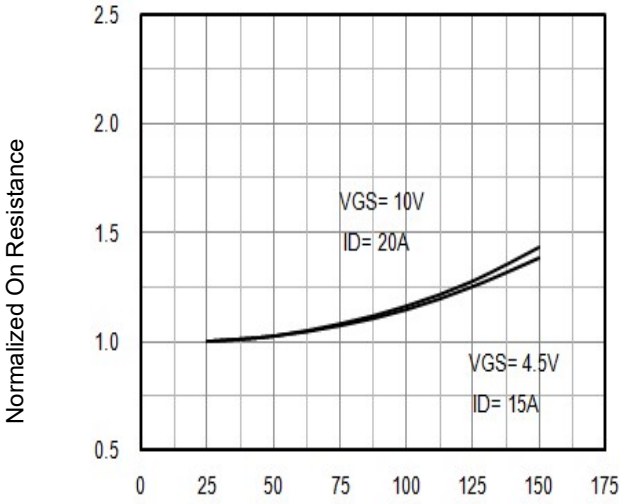


Fig4. Normalized On-Resistance Vs. Tj

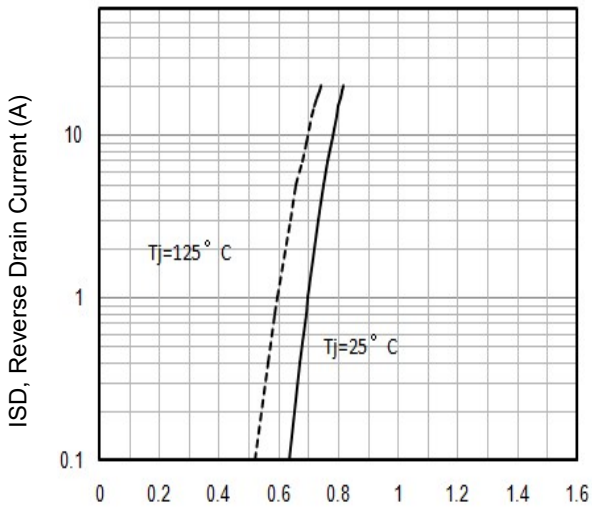


Fig5. Typical Source-Drain Diode Forward Voltage

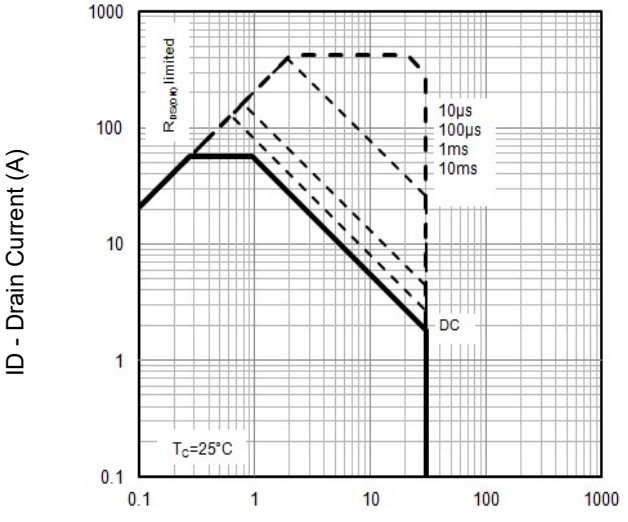


Fig6. Maximum Safe Operating Area

Typical Characteristics

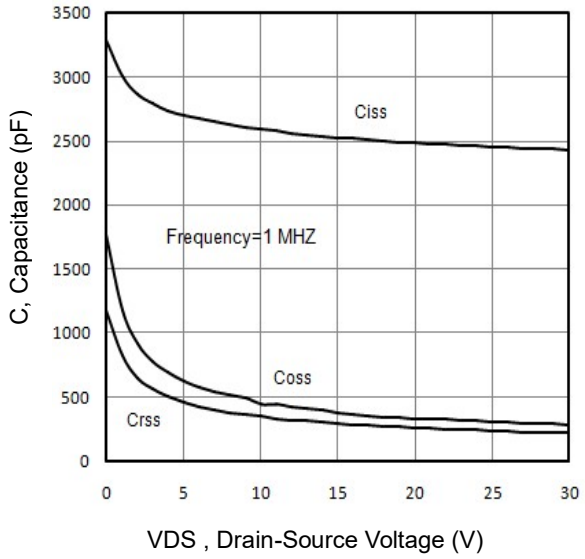


Fig7. Typical Capacitance Vs.Drain-Source Voltage

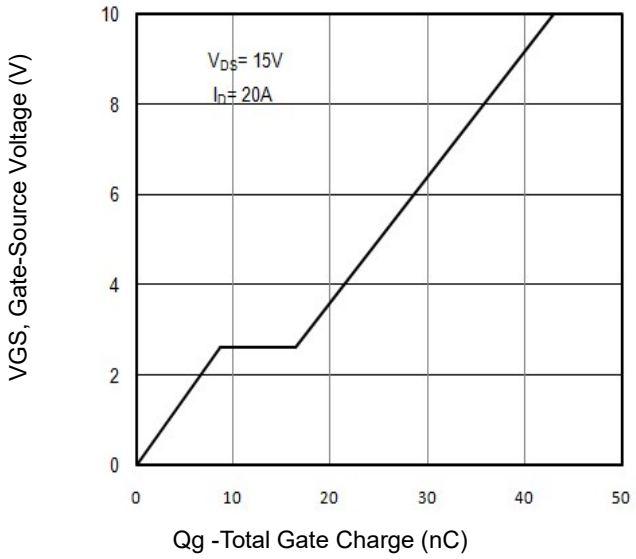


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

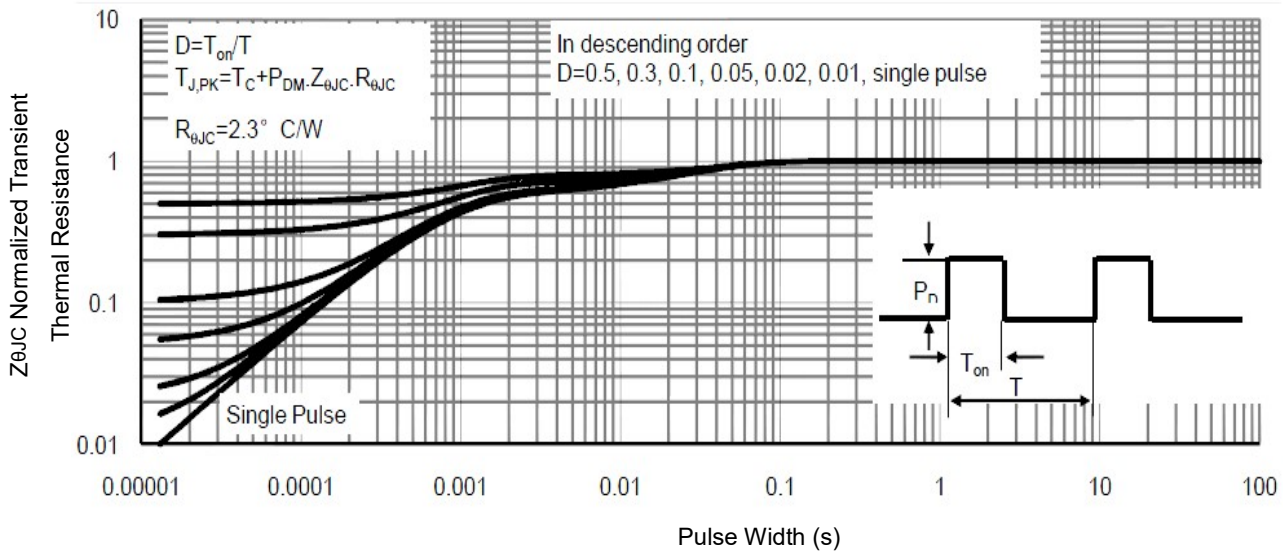


Fig9. Normalized Maximum Transient Thermal Impedance

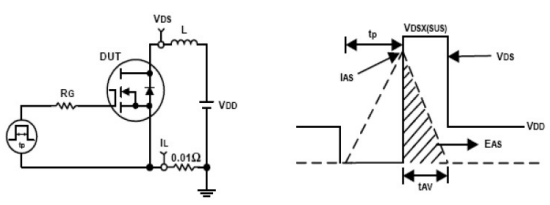


Fig10. Unclamped Inductive Test Circuit and waveforms

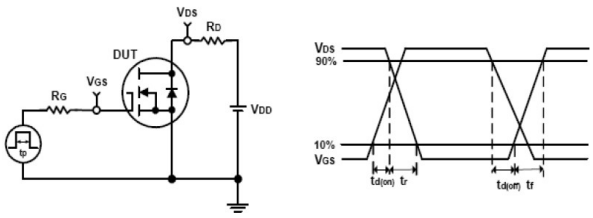
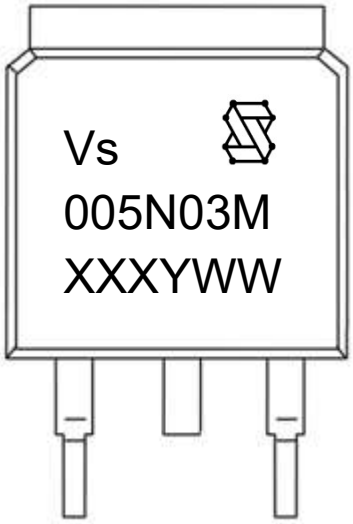


Fig11. Switching Time Test Circuit and waveforms

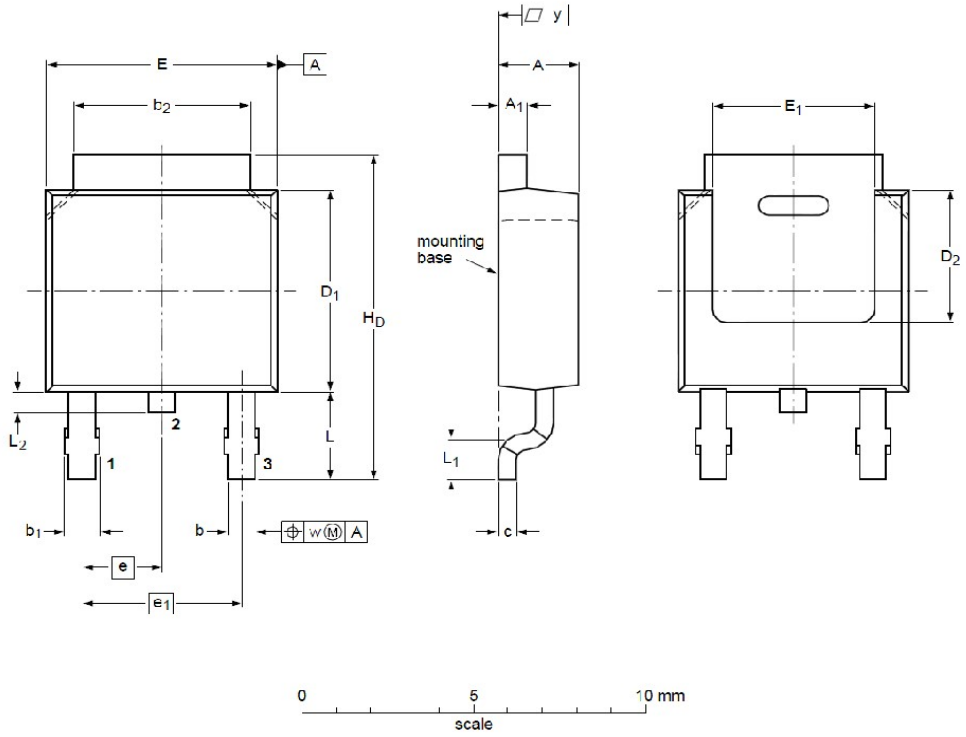
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（005N03M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	2.22	2.30	2.38	**A_1**	0.46	0.58	0.93
b	0.71	0.79	0.89	**b_1**	0.90	0.98	1.10
b_2	5.00	5.30	5.46	**c**	0.20	0.40	0.56
D_1	5.98	6.05	6.22	**D_2**	--	4.00	--
E	6.47	6.60	6.73	**E_1**	5.10	5.28	5.45
e	--	2.28	--	**e_1**	--	4.57	--
H_D	9.60	10.08	10.40	**L**	2.75	2.95	3.05
L_1	--	0.50	--	**L_2**	0.80	0.90	1.10
w	--	0.20	--	**y**	0.20	--	--

Customer Service

Sales and Service:
sales@vgsemi.com

Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: **www.vgsemi.com**