

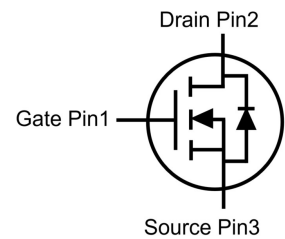
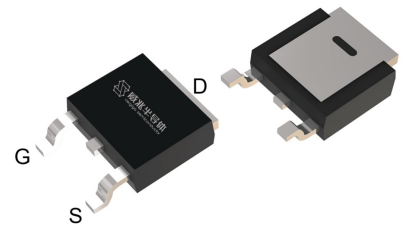
## Features

- Enhancement mode
- Low on-resistance  $R_{DS(on)}$  @  $V_{GS}=2.5\text{ V}$
- Fast Switching and High efficiency
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Packing
VS2622AD	TO-252	2622AD	2500pcs/Reel

$V_{DS}$	20	V
$R_{DS(on),TYP@ V_{GS}=4.5\text{ V}}$	6.5	m $\Omega$
$R_{DS(on),TYP@ V_{GS}=2.5\text{ V}}$	8.5	m $\Omega$
$I_D$	60	A

**TO-252**


## Maximum ratings, at $T_A = 25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	20	V
$V_{GS}$	Gate-Source voltage	$\pm 12$	V
$I_S$	Diode continuous forward current	$T_C = 25^\circ\text{C}$	60 A
$I_D$	Continuous drain current @ $V_{GS}=4.5\text{ V}$	$T_C = 25^\circ\text{C}$	60 A
		$T_C = 100^\circ\text{C}$	42 A
$I_{DM}$	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	240 A
$I_{DSM}$	Continuous drain current @ $V_{GS}=4.5\text{ V}$	$T_A = 25^\circ\text{C}$	10 A
		$T_A = 70^\circ\text{C}$	8 A
EAS	Avalanche energy, single pulsed ②	25	mJ
$P_D$	Maximum power dissipation	$T_C = 25^\circ\text{C}$	43 W
		$T_C = 100^\circ\text{C}$	21 W
$P_{DSM}$	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	1.25 W
		$T_A = 70^\circ\text{C}$	0.8 W
$T_{STG}, T_J$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

## Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ\text{C/W}$

**Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub>=25°C (unless otherwise stated)</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	--	--	100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.4	0.7	1.0	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	--	6.5	8.5	mΩ
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =3.3V, I <sub>D</sub> =6A	--	7.2	9.5	mΩ
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =2.5V, I <sub>D</sub> =4A	--	8.5	12	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz	1065	1255	1445	pF
C <sub>oss</sub>	Output Capacitance		165	195	225	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		140	165	190	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	--	1.7	--	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, I <sub>D</sub> =10A, V <sub>GS</sub> =4.5V	--	15	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	4.5	--	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =10V, I <sub>D</sub> =10A, R <sub>G</sub> =3Ω, V <sub>GS</sub> =10V	--	5.6	--	ns
t <sub>r</sub>	Turn-on Rise Time		--	41	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	30	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	17	--	ns
<b>Source- Drain Diode Characteristics@ T<sub>j</sub>= 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =10A, V <sub>GS</sub> =0V	--	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>j</sub> =25°C, I <sub>sd</sub> =10A, V <sub>GS</sub> =0V	--	13	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	--	3.7	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 10A, V<sub>GS</sub> = 4.5V. Part not recommended for use above this value
- ③ The power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

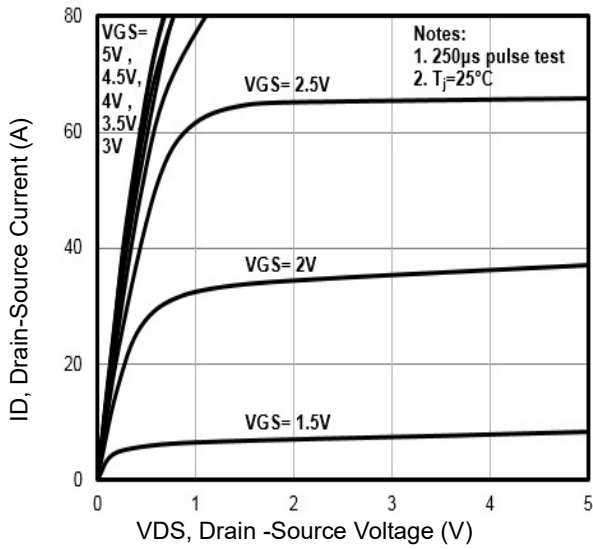


Fig1. Typical Output Characteristics

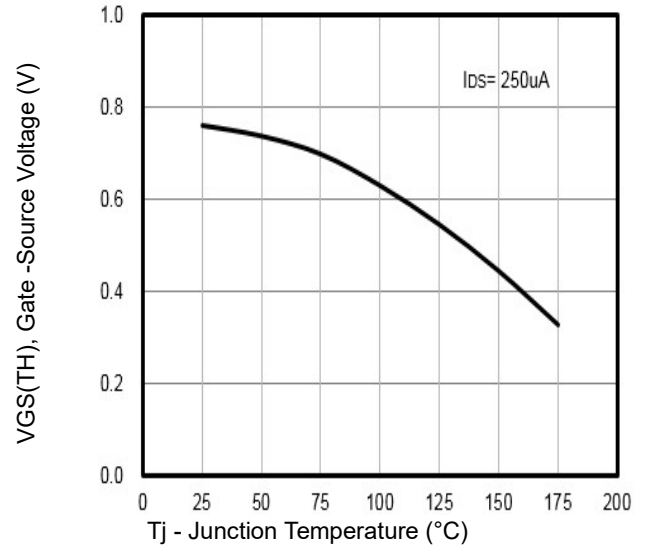


Fig2.  $V_{GS(TH)}$  Gate -Source Voltage Vs.  $T_j$

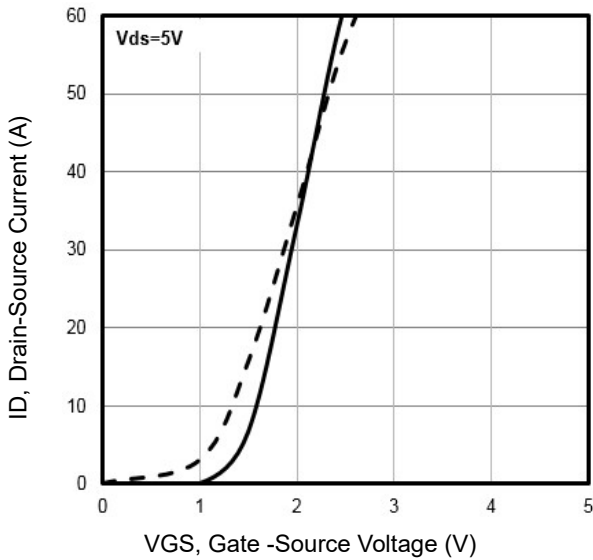


Fig3. Typical Transfer Characteristics

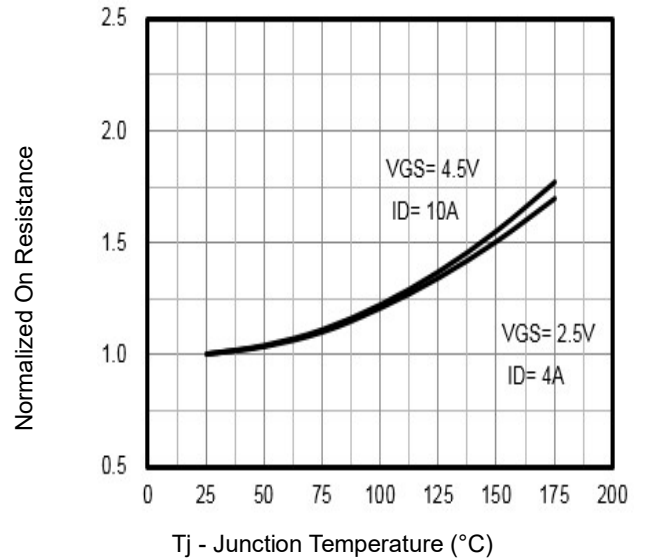


Fig4. Normalized On-Resistance Vs.  $T_j$

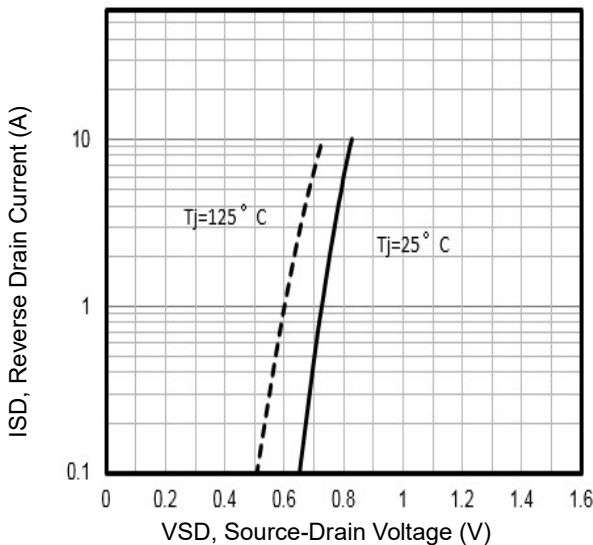


Fig5. Typical Source-Drain Diode Forward Voltage

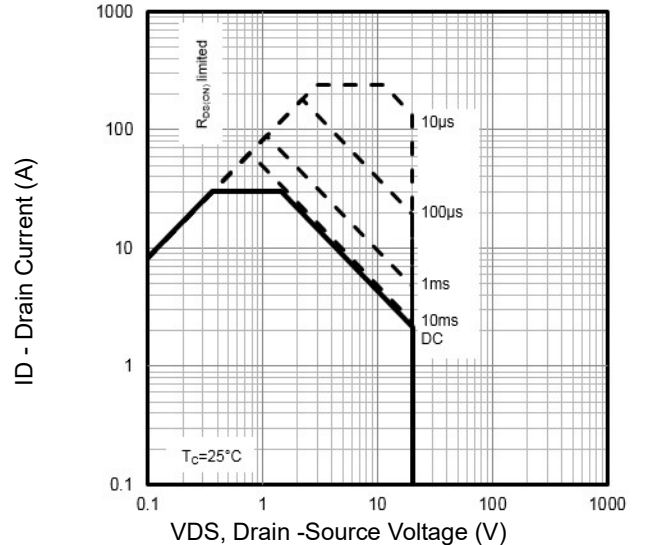
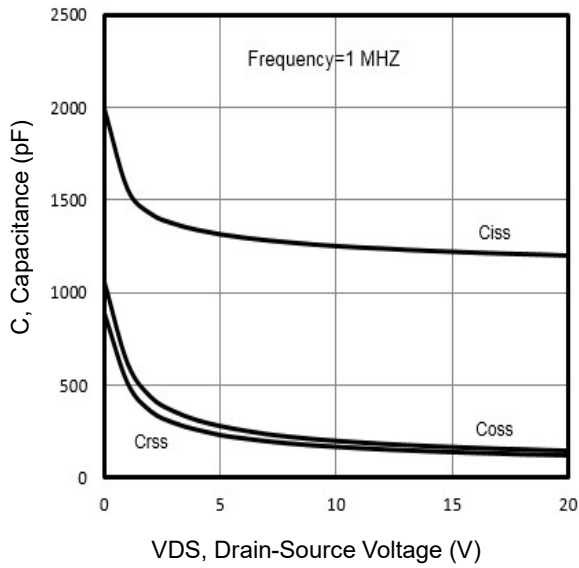
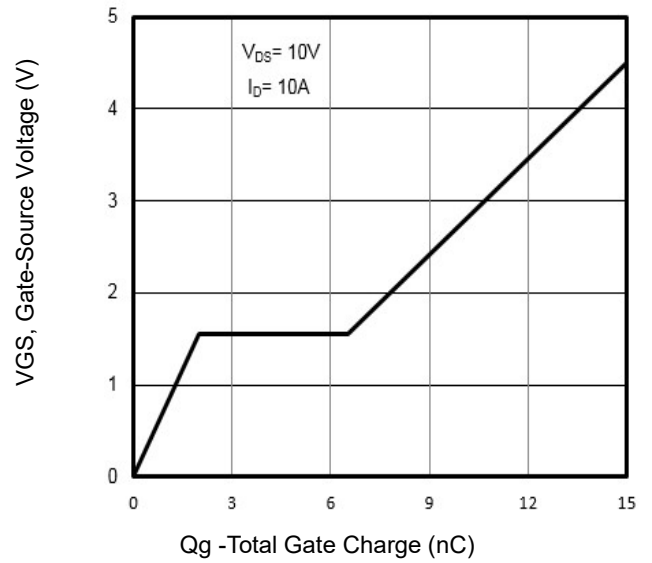


Fig6. Maximum Safe Operating Area

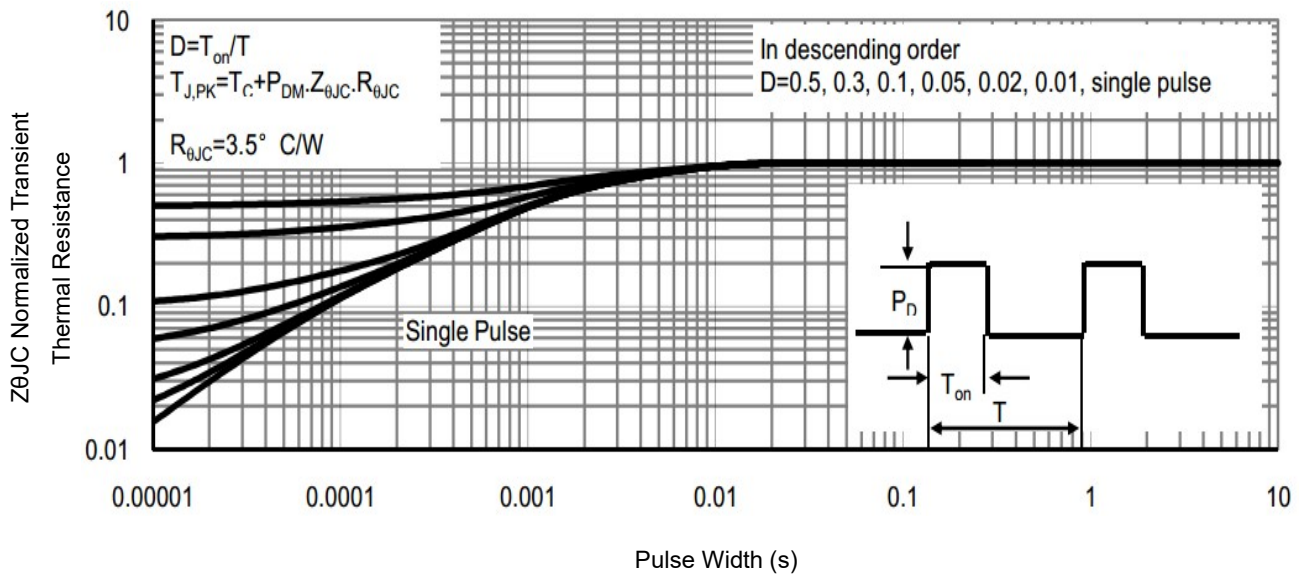
**Typical Characteristics**



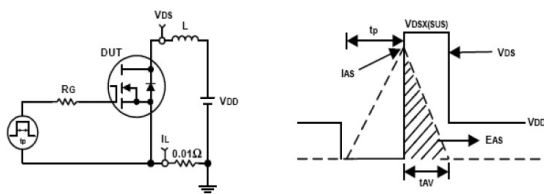
**Fig7.** Typical Capacitance Vs. Drain-Source Voltage



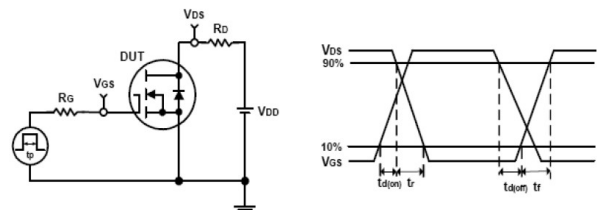
**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage



**Fig9.** Normalized Maximum Transient Thermal Impedance

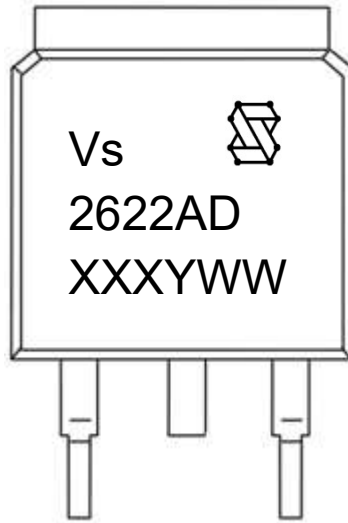


**Fig10.** Unclamped Inductive Test Circuit and waveforms



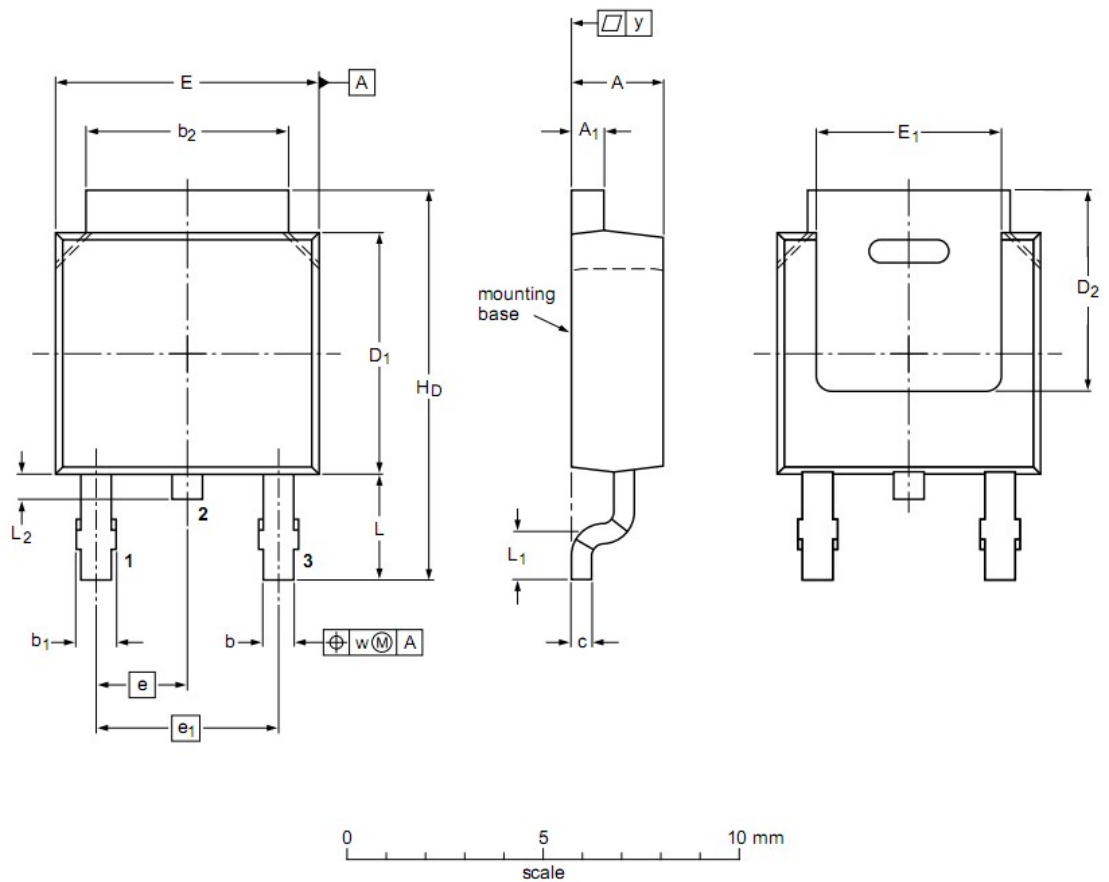
**Fig11.** Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs) , Vergiga Logo
- 2nd line: Part Number (2622AD)
- 3rd line: Date code (XXXYWW)
  - XXX: Wafer Lot Number Code , code changed with Lot Number
  - Y: Year Code , refer to table below
  - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

**TO-252 Package Outline Data**


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
<b>A</b>	2.20	2.30	2.38
<b>A<sub>1</sub></b>	0.46	0.50	0.63
<b>b</b>	0.64	0.76	0.89
<b>b<sub>1</sub></b>	0.77	0.85	1.14
<b>b<sub>2</sub></b>	5.00	5.33	5.46
<b>c</b>	0.458	0.508	0.558
<b>D<sub>1</sub></b>	5.98	6.10	6.223
<b>D<sub>2</sub></b>	5.21	--	--
<b>E</b>	6.40	6.60	6.731
<b>E<sub>1</sub></b>	4.40	--	--
<b>e</b>	2.286 BSC		
<b>e<sub>1</sub></b>	--	4.57	--
<b>H<sub>D</sub></b>	9.40	10.00	10.40
<b>L</b>	2.743 REF		
<b>L<sub>1</sub></b>	1.40	1.52	1.77
<b>L<sub>2</sub></b>	0.50	0.80	1.01
<b>w</b>	--	0.20	--
<b>y</b>	--	--	0.20

**Notes:**

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

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